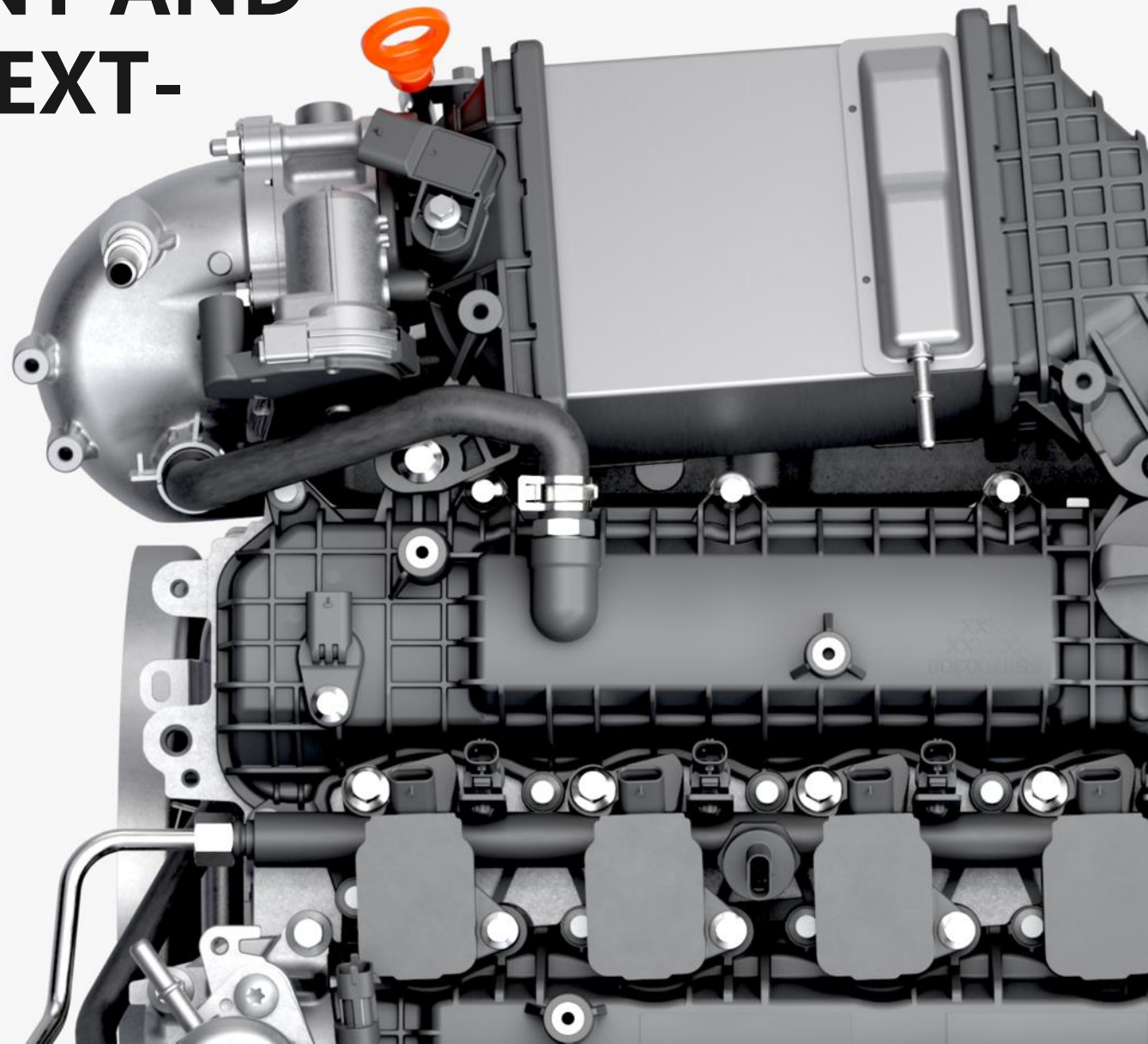


PCB EMBEDDED GAN POWER MODULE DEVELOPMENT AND ITS APPLICATION IN NEXT- GENERATION HYBRID SYSTEMS

Advanced Technology & Strategy Center

Yongquan MA, Dr.

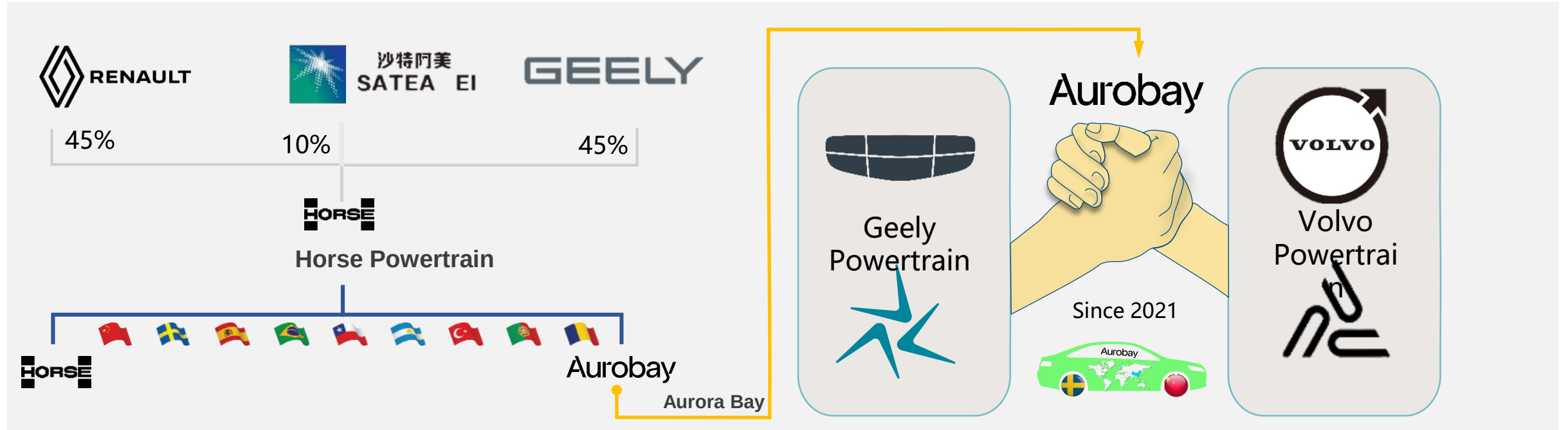
3 Oct.,2026, Aachen



Horse Powertrain, Who are we?

■ Vision: Revolutionizing motion for all

- On 31st May, 2024, Geely and Renault joined forces to officially establish Horse Powertrain.



€15B
Revenue Outlook



18
Manufactur
ing Bases



5 R&D
Centers



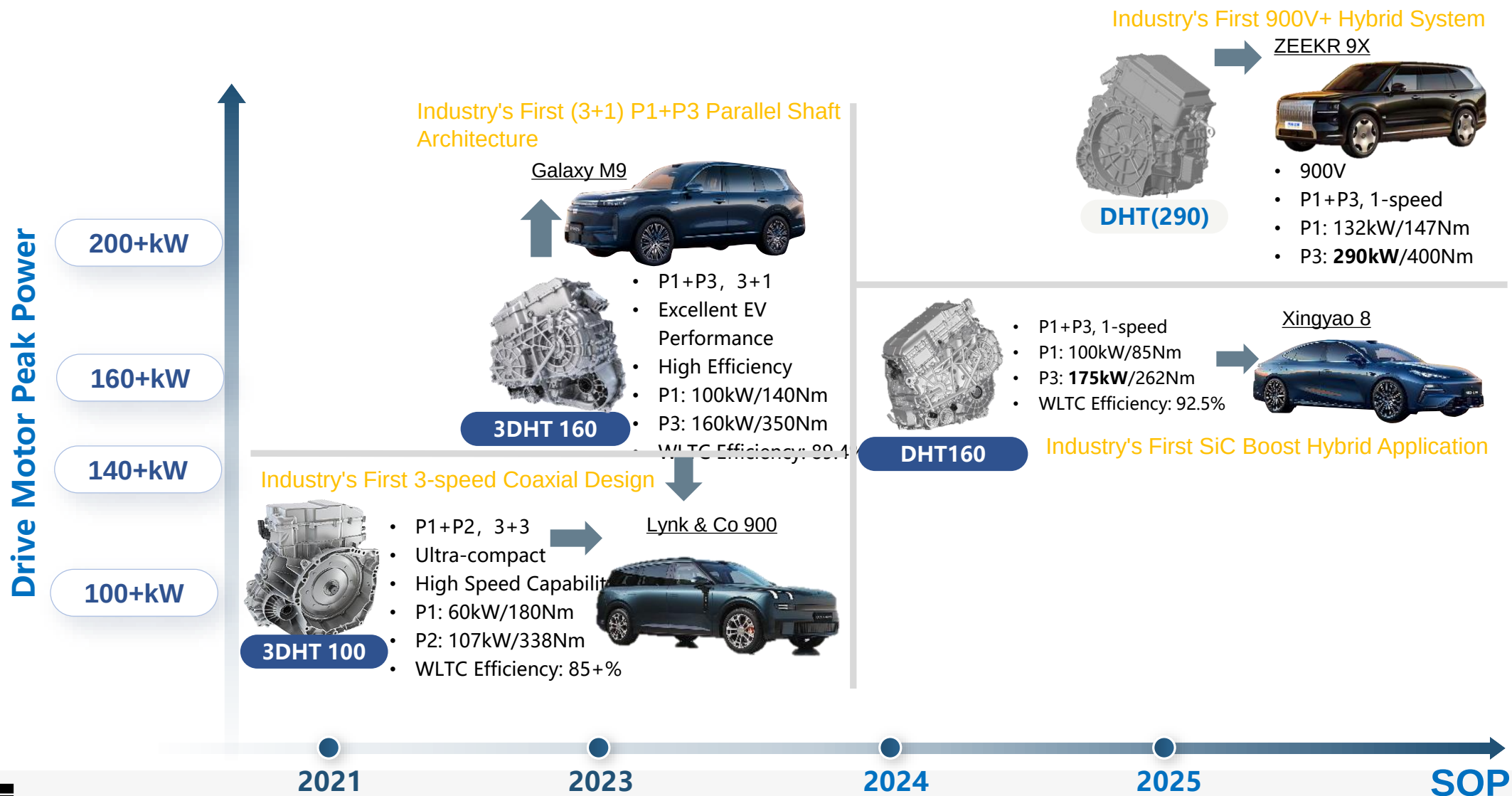
8M Units
Annual Engine &
Transmission Output



19,000
Employees

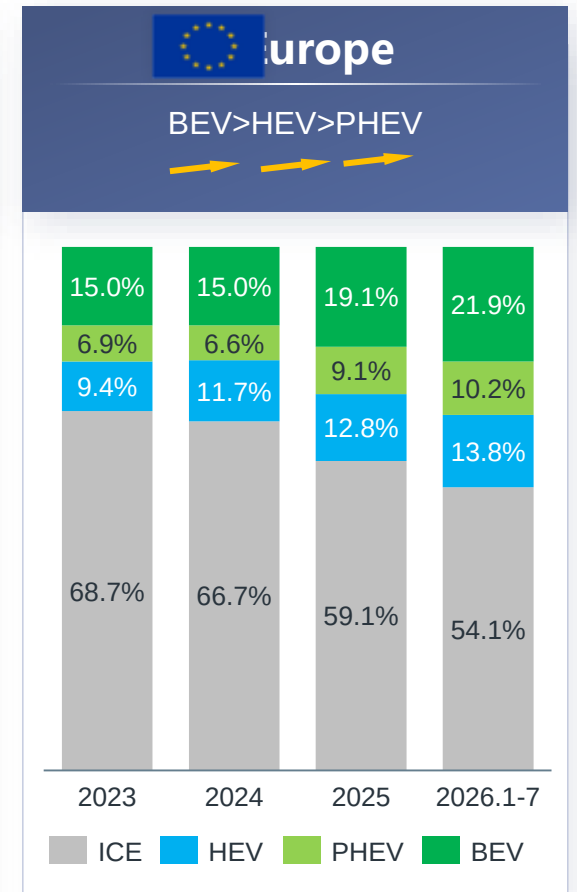
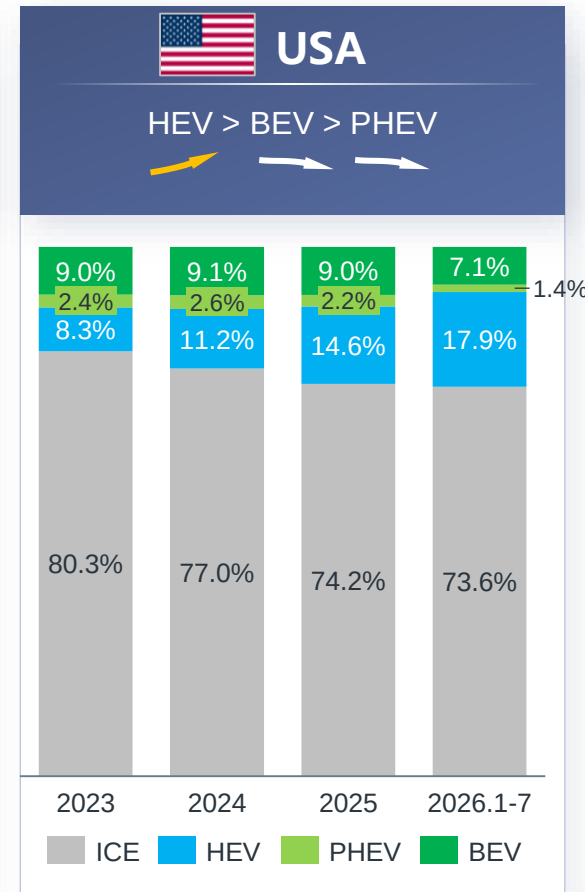
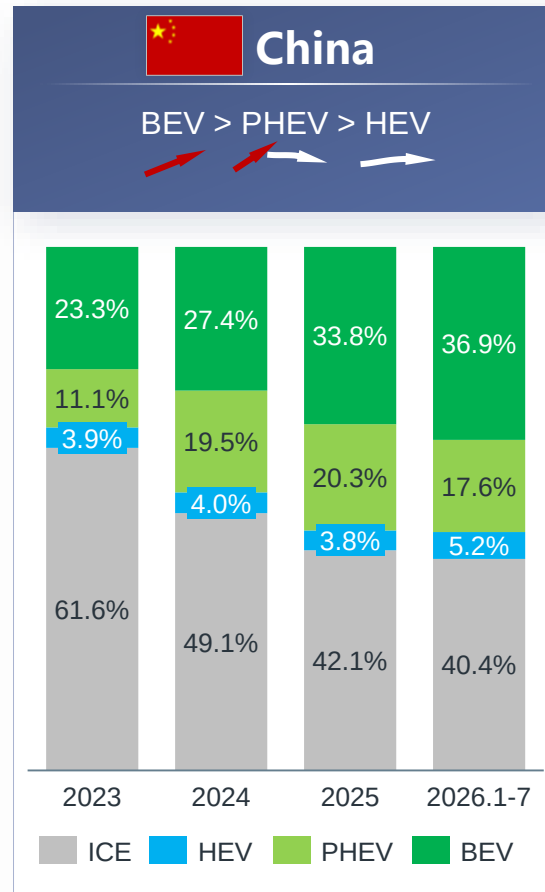
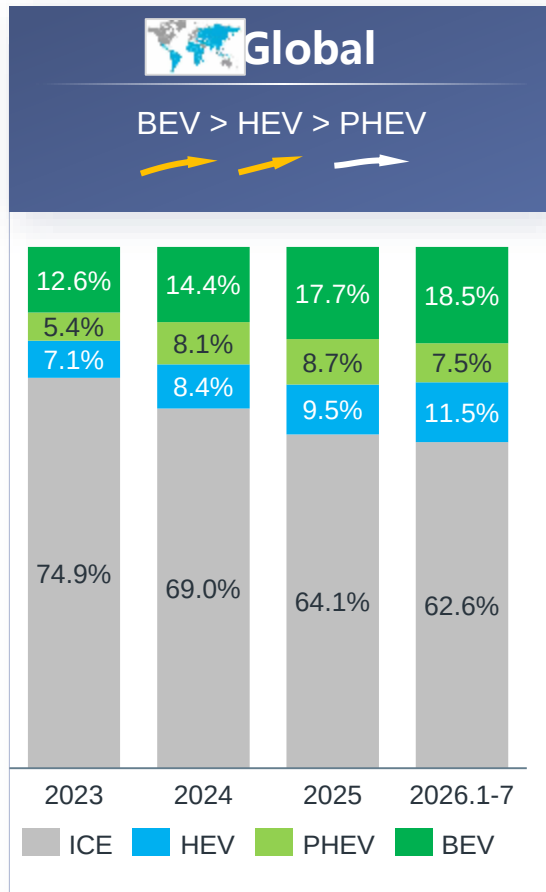
Horse Powertrain Hybrid System Development Practice

- P1+P2/P3, 100kW-290kW, 1/3-speed, 400V/800V, HEV/PHEV/REEV.



Global Passenger Car Powertrain Market Trend Analysis

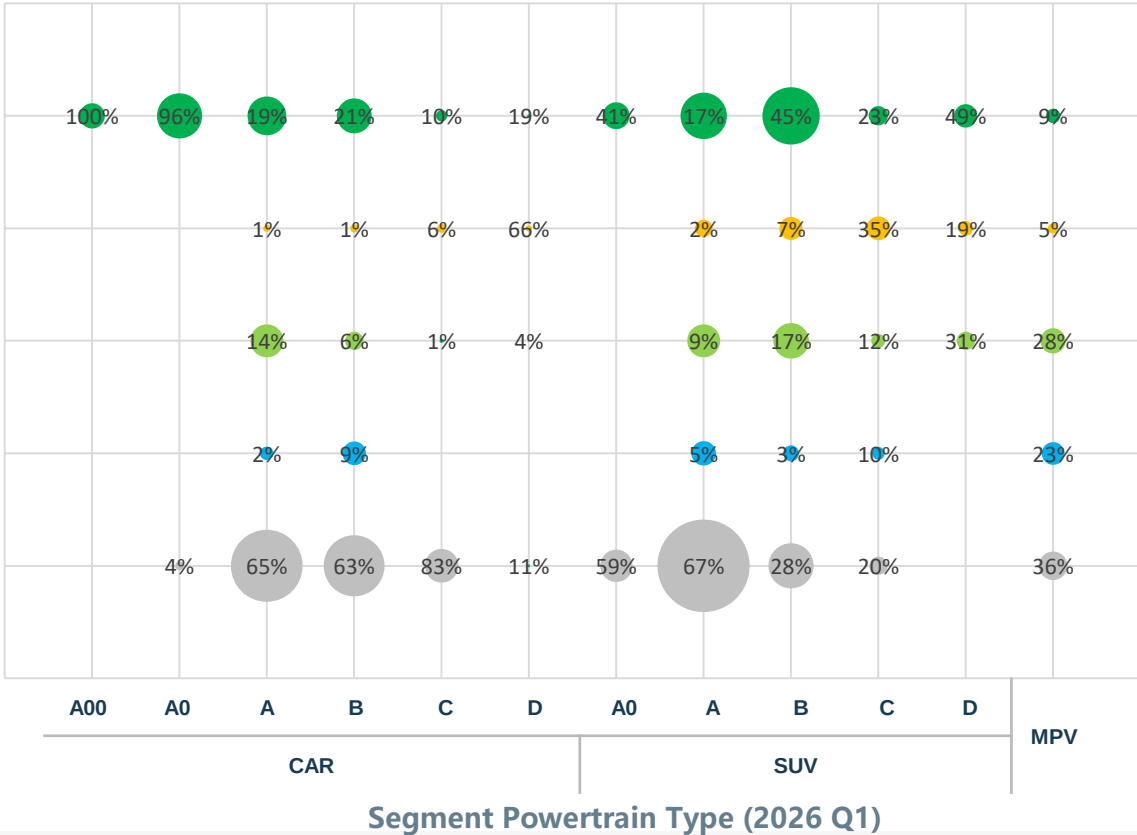
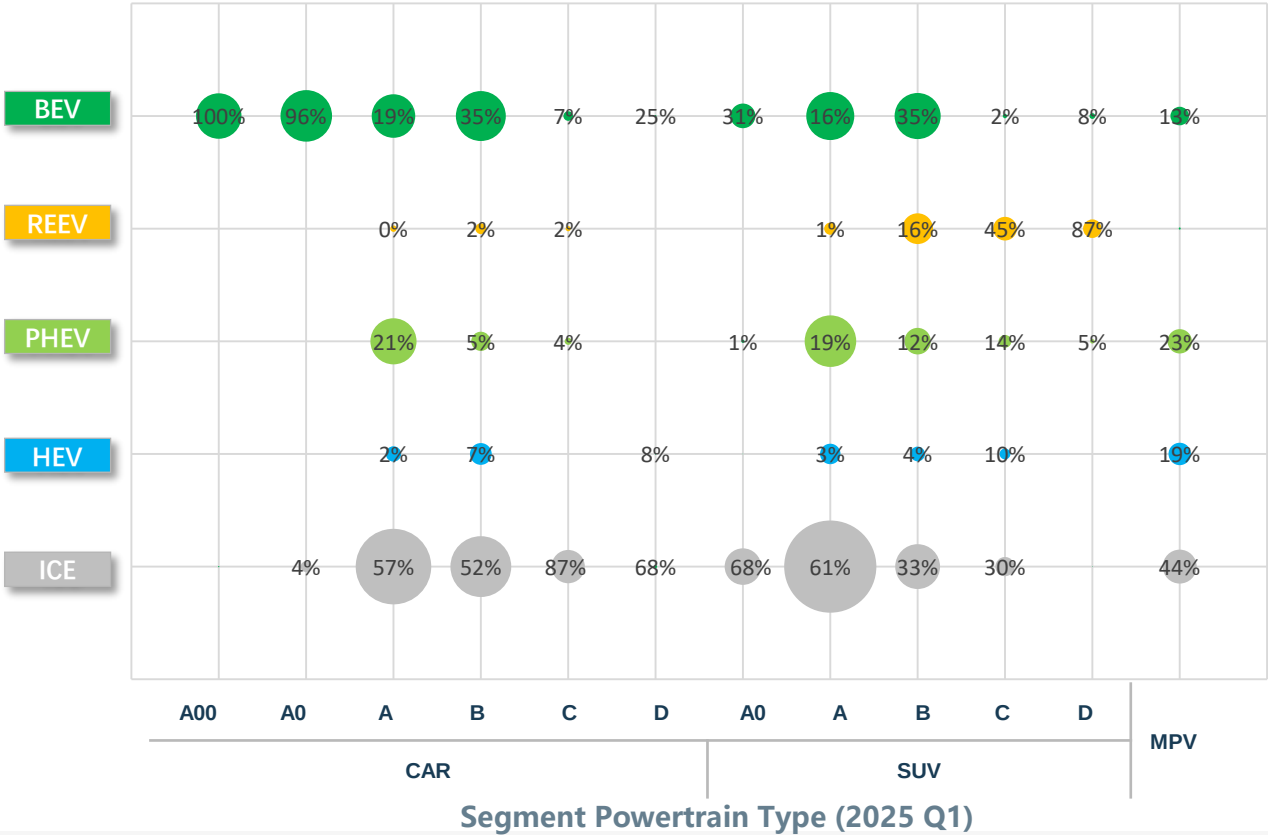
- Global passenger car electrified powertrain (xEV) continues to grow, but with significant regional divergence;
- China driven by BEV and PHEV, xEV share reached 60% by July 2026, surpassing ICE. US ICE share remains high, HEV growing fastest; Europe shows policy-driven steady electrification, BEV rising to 22%, with HEV and PHEV maintaining balanced growth.



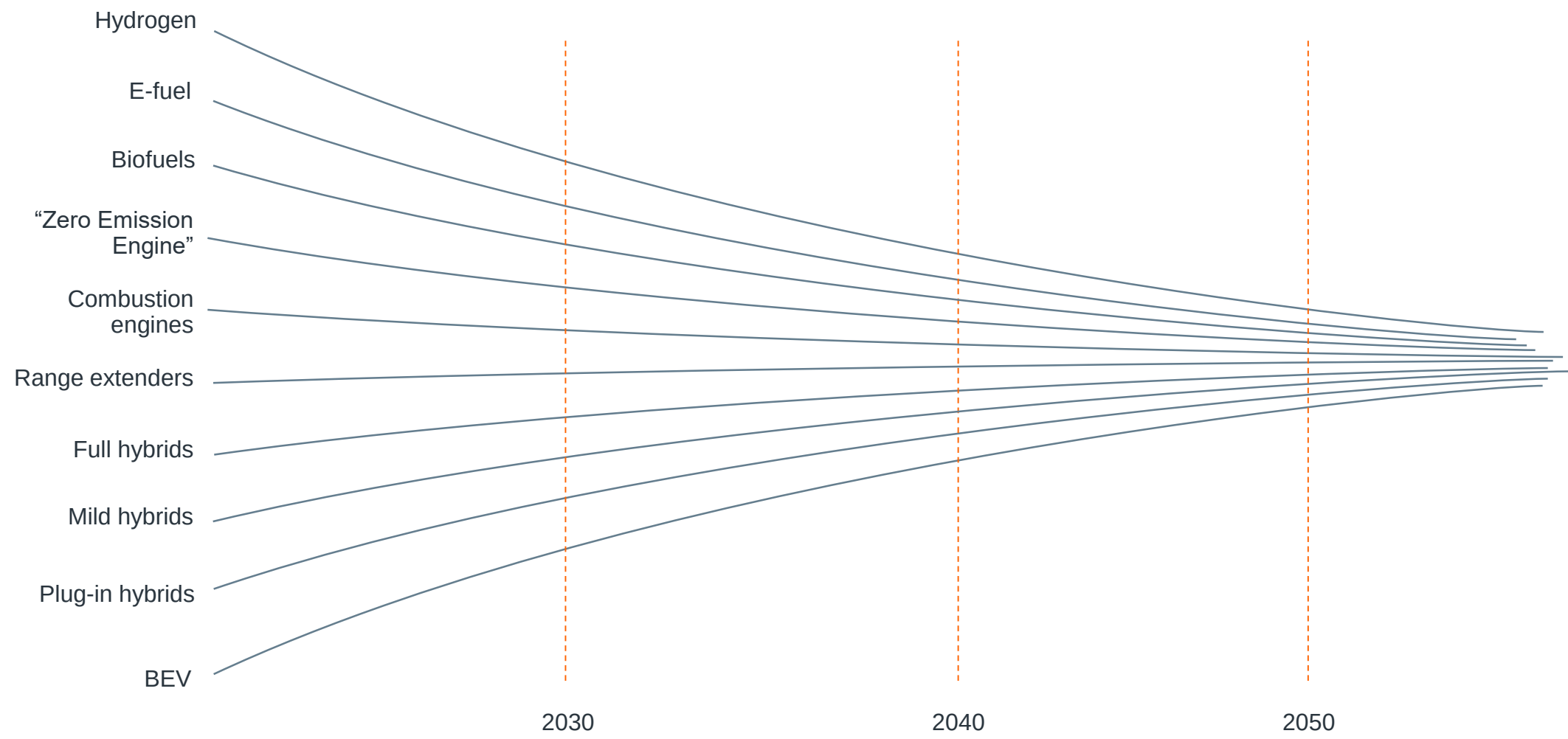
Source: S&P Global Passenger Car Database; Retail volumes

China Market Powertrain Type Distribution

- BEV: Dominates small car market with near 100% penetration. B/D-segment sedans declined YoY. Growth in mid/large SUVs; premium BEV SUV market rapidly opening;
- REEV: D-segment sedans grew, D-segment SUVs declined. Users shifting to BEV/PHEV; structural adjustment in mid-large SUVs;
- PHEV: Strong growth in D-segment SUVs, declined in A-segment sedans;
- HEV: Unexpected growth in MPV market; becoming optimal transition for ICE owners upgrading to MPV

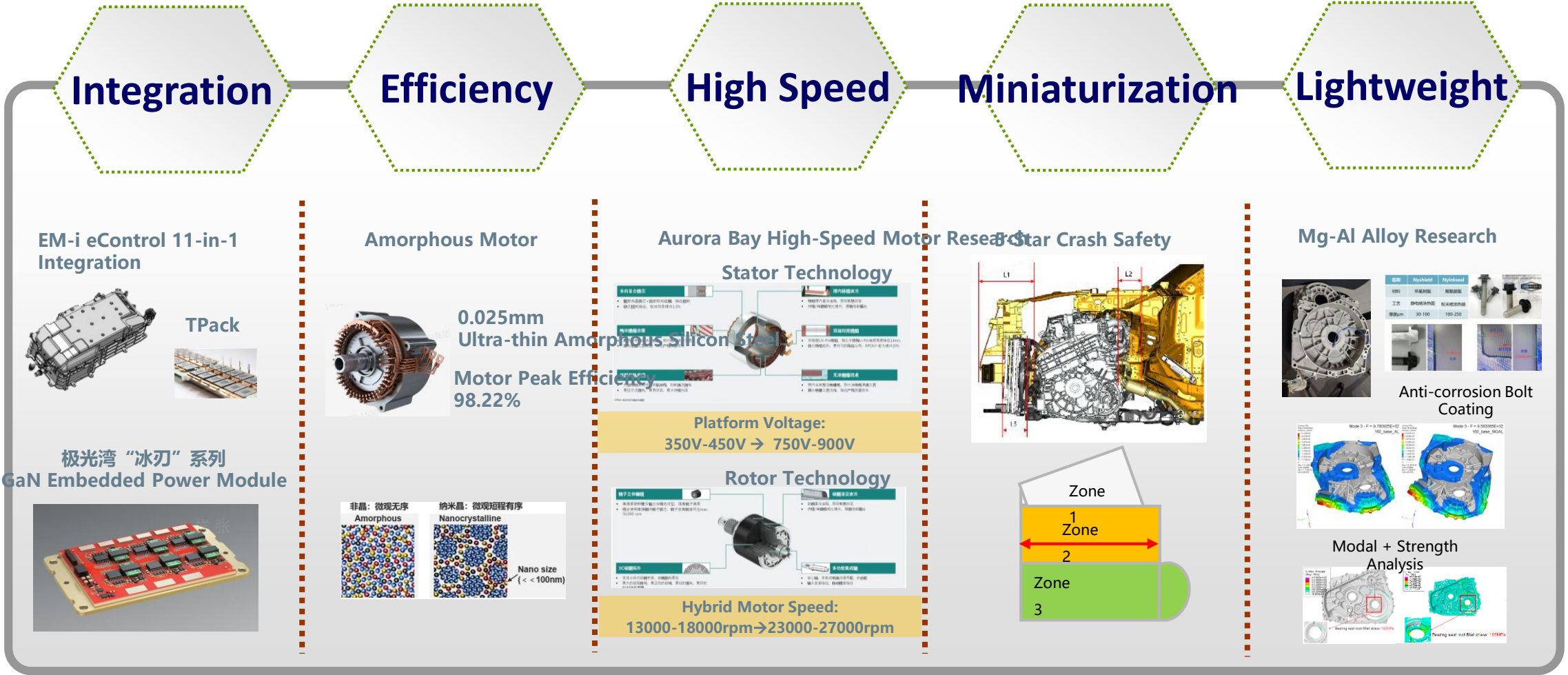


Achieving Net-Zero: Pure Electric Is Not the Only Path



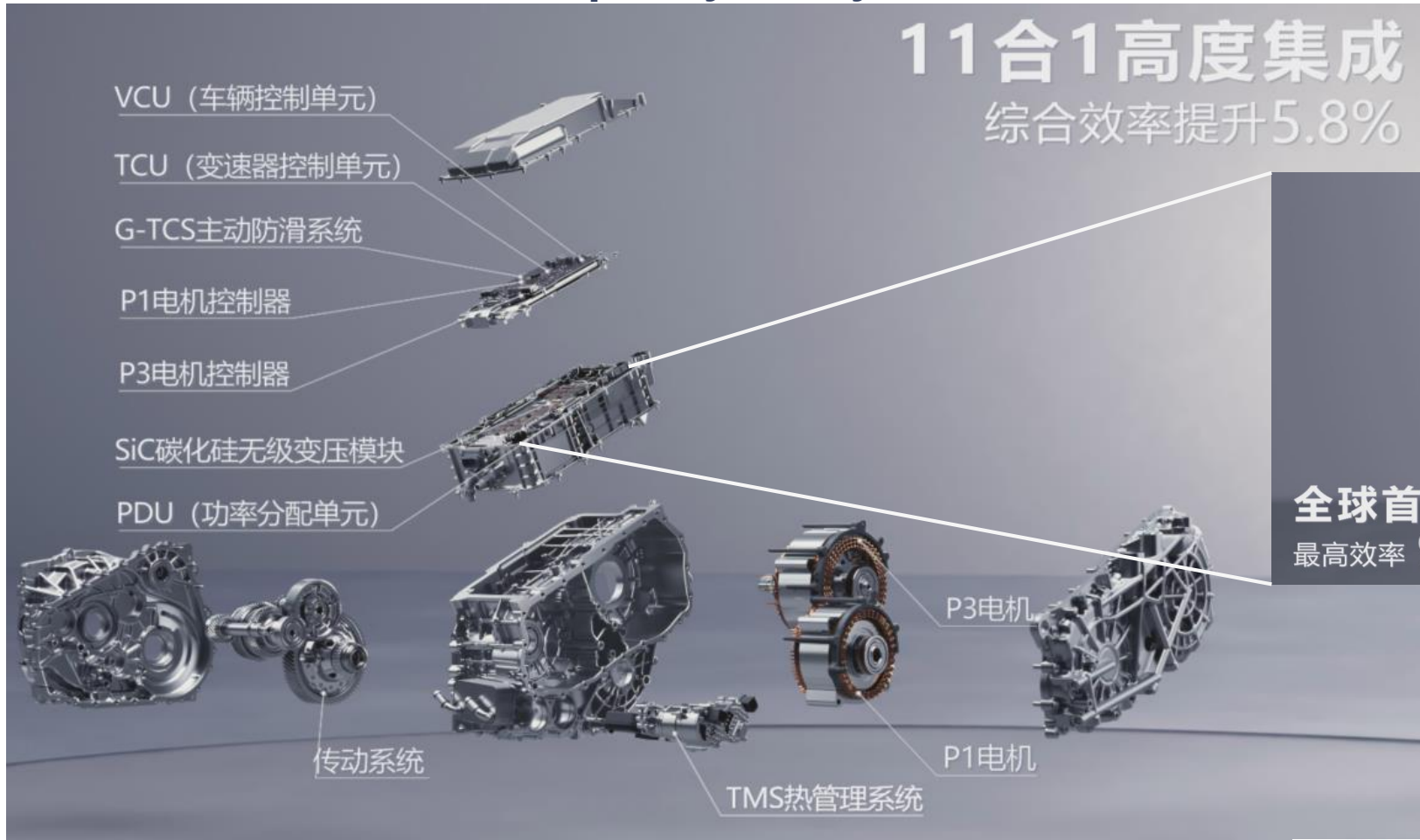
Hybrid Powertrain Challenges: Efficiency, Size, Cost

- Hybrid Powertrain System Trends: Integration, Platformization, High Efficiency, High Speed, High Voltage, Miniaturization, Lightweight.



Hybrid Powertrain Challenges: Efficiency, Size, Cost

HORSE Super Hybrid System



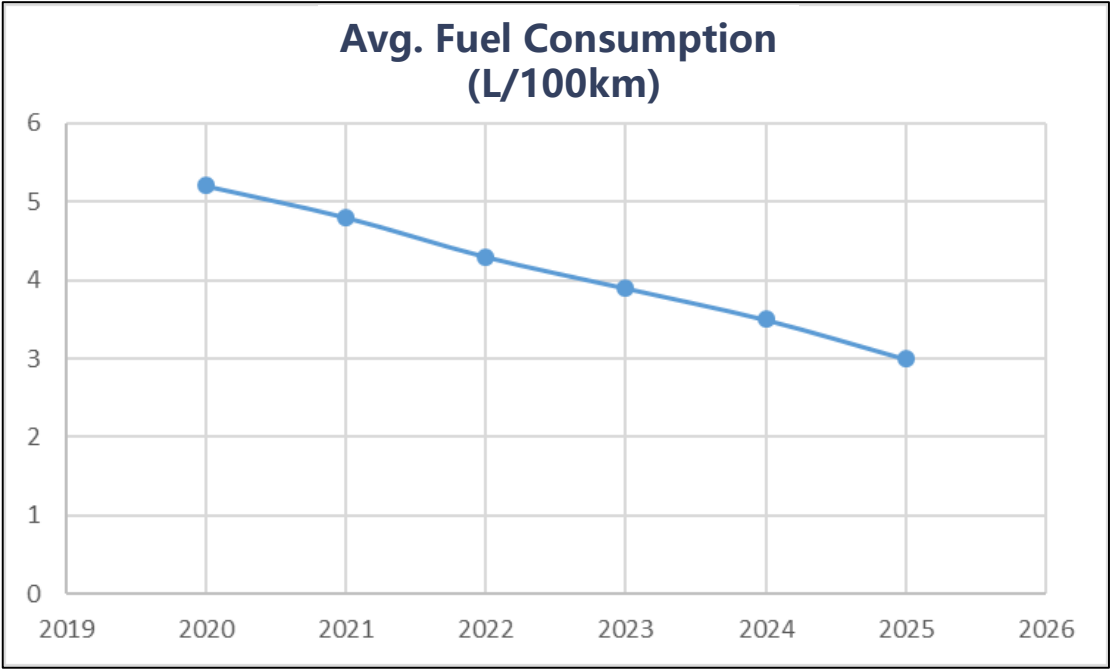
- Power Modules: Can SiC costs reduced to silicon IGBT levels?
- 5-Star Crash Design: Can multi-in-one integration reduce size further?
- Where should the optimization of volume, density, cost for HORSE Hybrid go?



Hybrid Powertrain Challenges: Efficiency, Size, Cost

HORSE Super Hybrid Efficiency Evolution

Year	Avg. Fuel Consumption (L/100km)	Key Tech Milestones
2020	5.2	1st-gen Thunder PHEV, 1.5T + single motor
2021	4.8	Optimized e-control logic, increased EV range
2022	4.3	2nd-gen system, 3-speed DHT Pro transmission
2023	3.9	44% thermal efficiency engine, improved battery density
2024	3.5	Smart energy recovery + predictive energy management
2025	3.0	Full-range 800V + SiC electric drive



- HORSE hybrid fuel consumption declining rate about 0.44L/Year;
- HV E/E system efficiency approaching the limits of Si-based IGBT ;
- Where should the optimization of efficiency for HORSE hybrid go?

Next-Gen Power Electronics Technology Trends

EU HiEFFICIENT Project

- EU focusing on the greenhouse gas emission neutrality targets set out in the European Green Deal, launched the “HiEFFICIENT” next-generation power electronics development program. This program aims to develop highly reliable, integrated wide-bandgap power semiconductor technologies for energy-efficient, carbon-neutral transportation systems and to apply them to the drive, testing, and charging infrastructure of electric vehicles.
- Among the seven key task objectives of the program, it explicitly proposes the development of gallium nitride (GaN)-based system-on-chip (SoC) solutions, and in particular sets out the development task of embedding and integrating bare dies of wide-bandgap semiconductor devices such as GaN and SiC into PCBs.
- Among the six key application scenarios of the program, it explicitly proposes adopting integrated packaging technology with GaN embedded in PCBs for automotive electric powertrain inverters, OBCs, and DC-DC converters.
- The participating organizations of the program include major renowned universities, research institutions, and enterprises across the EU.

WP1 - Use case specification, and KPI evaluation

WP2 - GaN SoC and SiP integration and embedded technologies

WP3 - Design optimization for reliable power electronic systems and virtual prototyping



WP2 pursues the overall target of providing novel integrated GaN components for efficiency and power density. This work package will address rating switches with drivers in diverse concepts such as SiP and reduce parasitic loop inductances. In the 100 V integrated GaN early lagging behind the developments of US companies and catch up, which should be possible with the envisioned GaN-SiP, the planned GaN-SoC integration will set a new benchmarking losses. In addition to the 100 V activities, a 650 V GaN-SoC will be developed which would be the world-wide first GaN-configuration in one semiconductor. Being complemented by adding technologies including many aspects (e.g., material considerations) and a dedicated tasks dealing with reliability and optimized to contribute to three use cases as well as the highly targeted goals.

With other WPs: WP1 and WP5, vertically with WP3 and WP4

PROJECT PARTNERS

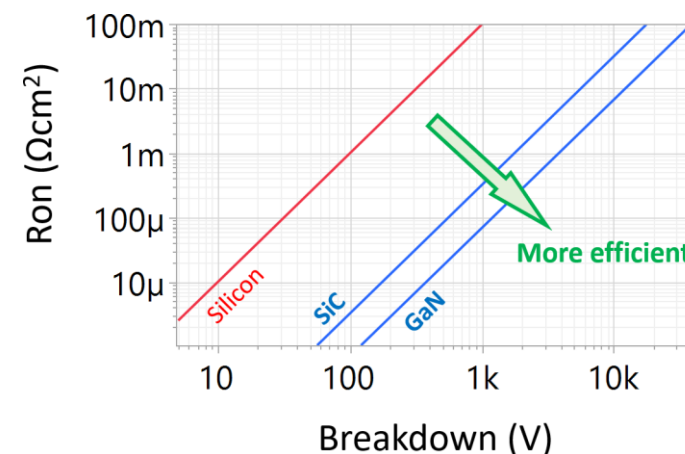
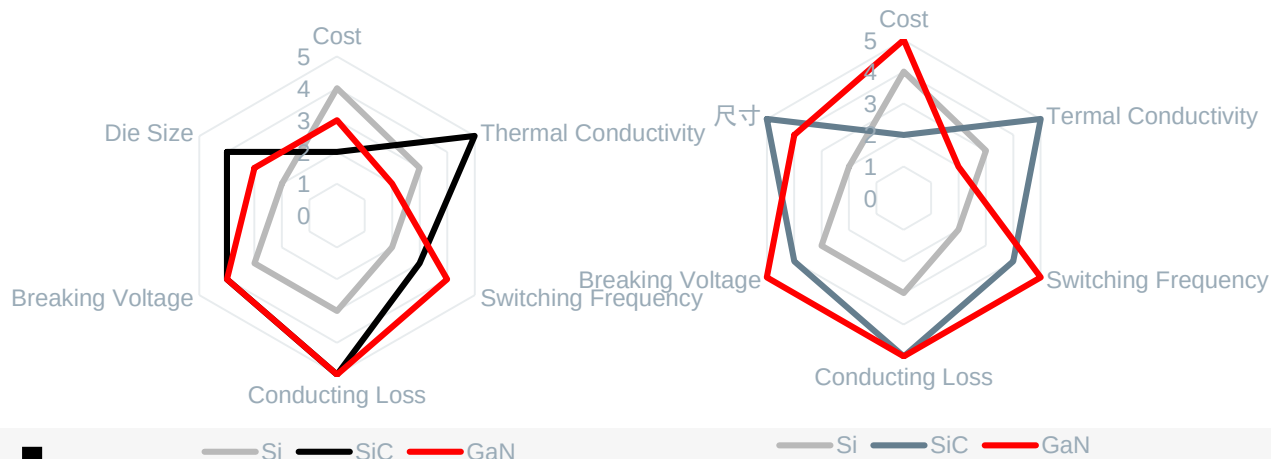


Next-Gen Power Electronics Technology Trends

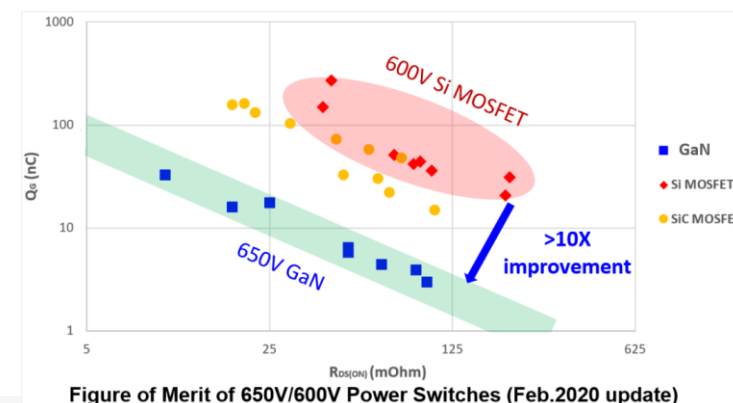
GaN Advantages over Si/SiC:

- GaN, a 3rd-gen semiconductor, has wider bandgap, higher critical breakdown field and electron mobility than Si/SiC. Higher mobility means faster switching and lower losses, i.e., higher efficiency and power density.
- From material perspective, GaN specific on-resistance is one order of magnitude lower than SiC, and FOM($R_{\text{dson}} \cdot Q_g$) also surpasses SiC; however thermal stability remains a challenge;

Property	Si	SiC	GaN
Bandgap (eV)	1.12	3.3	3.44
Critical Breakdown Field (V/cm)($\times 10^6$)	0.3	2-4	3.3
Electron Mobility (cm^2/Vs)	1000-1400	800-1200	1500-2000
Saturation Velocity (cm/s)($\times 10^7$)	1	2	2.2
Thermal Conductivity (W/cm ² K)	1.5	4.9 未来	1.3-2.2



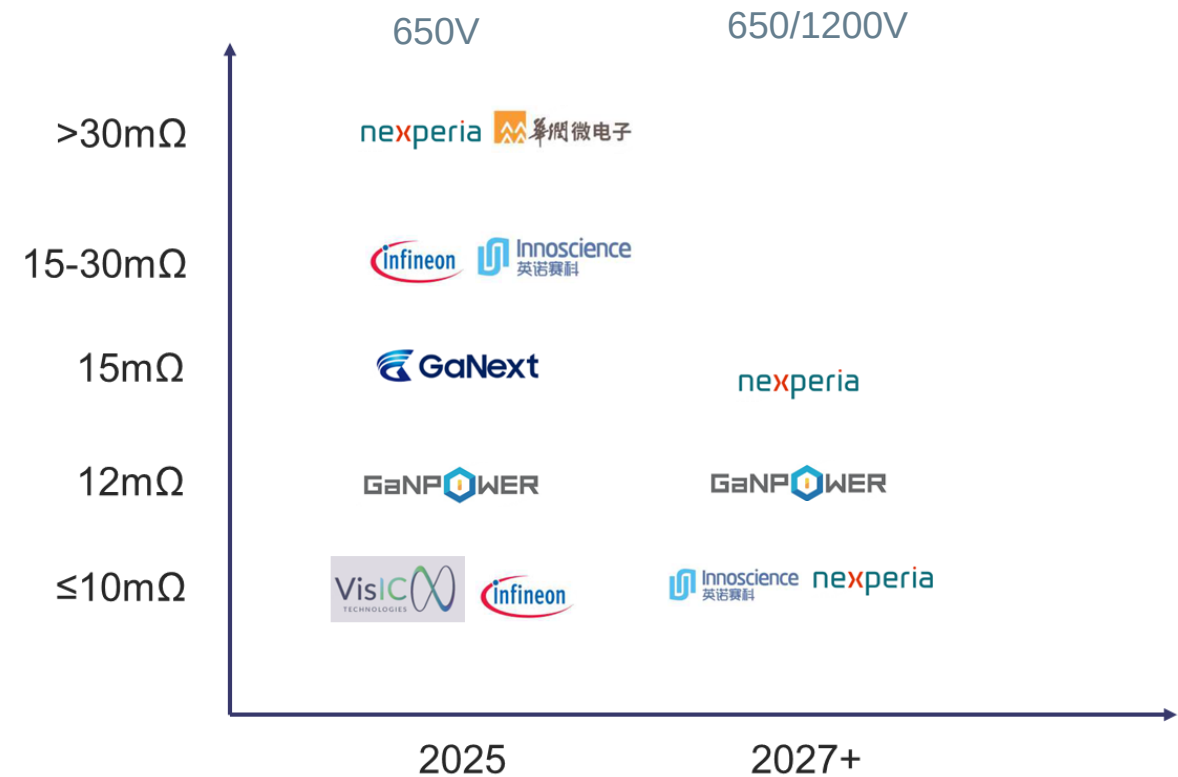
On-resistance comparison: x-axis=breakdown voltage, y-axis=specific on-resistance



FOM comparison: x-axis=on-resistance, y-axis=gate charge (switching loss)

Power GaN Development Status & Trends

- GaN HEMT trends: E-mode (normally-off) and D-mode (normally-on) designs developing in parallel, progressively improving voltage rating and integration, reducing high-temp Rdson, enhancing current control reliability, developing composite substrate tech, and establishing specific automotive test standards.

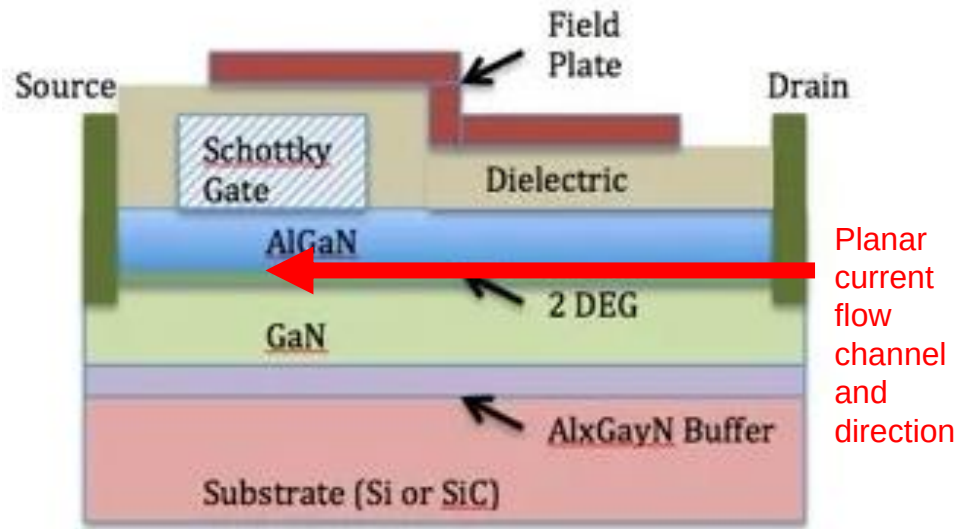


	Enhancement-mode E-Mode	Normally-off Depletion D-Mode
Description	Directly modifies gate structure	Gate structure unchanged
Key Advantages	Better performance, smaller device size	High voltage, high reliability, standard MOS gate drive, easy high-power design
Key Disadvantages	Narrow gate drive range, low voltage, lower reliability, immature process, incompatible with existing drivers;	Relatively lower performance, needs additional Si MOS, larger chip size;
Key Manufacturers	Infineon (incl. GaN Systems), EPC, GaN Power, Navitas, Panasonic, Innoscience, Chengdu Navitas, etc.	VisiC, Transphorm, PI, TI, Nexperia, GaN Future, Runxin Micro, etc.
Typical Solutions	Single-device E-mode (P-GaN): P-type GaN epitaxial layer at gate for turn-off control.	Cascode structure: integrates a low-voltage E-mode N-ch MOS for normally-off, switching via the series MOS.

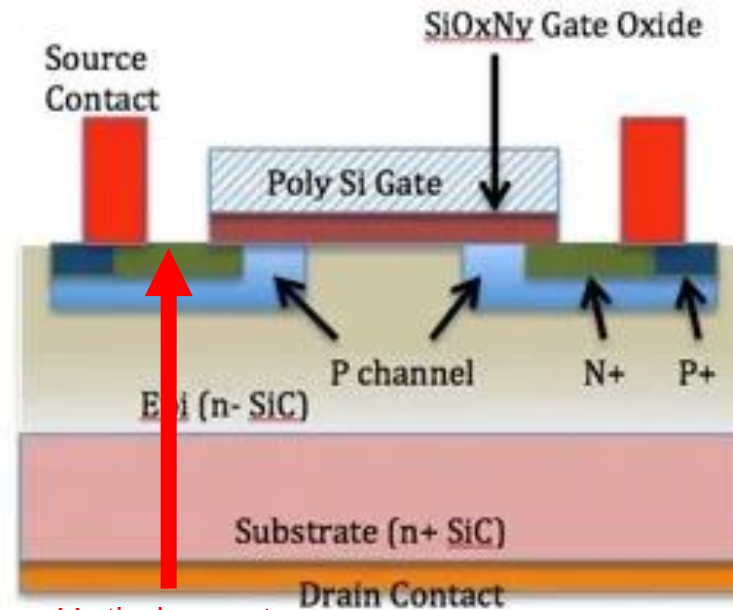
Power GaN Development Status & Trends

Current Key Issues with GaN:

- GaN HEMT uses Si substrate (GaN-on-Si) for cost reduction; the Si-GaN heterojunction is prone to lattice mismatch during epitaxial growth;
- Lattice mismatch induces interface and bulk defects, causing dynamic $R_{ds(on)}$ degradation at high temperature. Combined with GaN's low thermal conductivity, GaN-on-Si devices are prone to high-temp performance degradation, durability loss, and thermal runaway;
- GaN-on-Si HEMT uses planar structure, unlike the vertical structure common in IGBT and SiC MOSFET, resulting in larger specific current-carrying area;



GaN HEMT Planar Structure



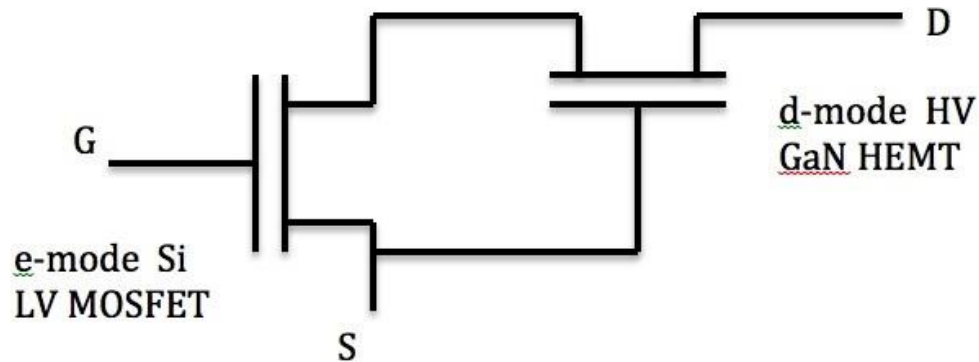
Vertical current
flow channel
and direction

SiC VDMOS Vertical Structure

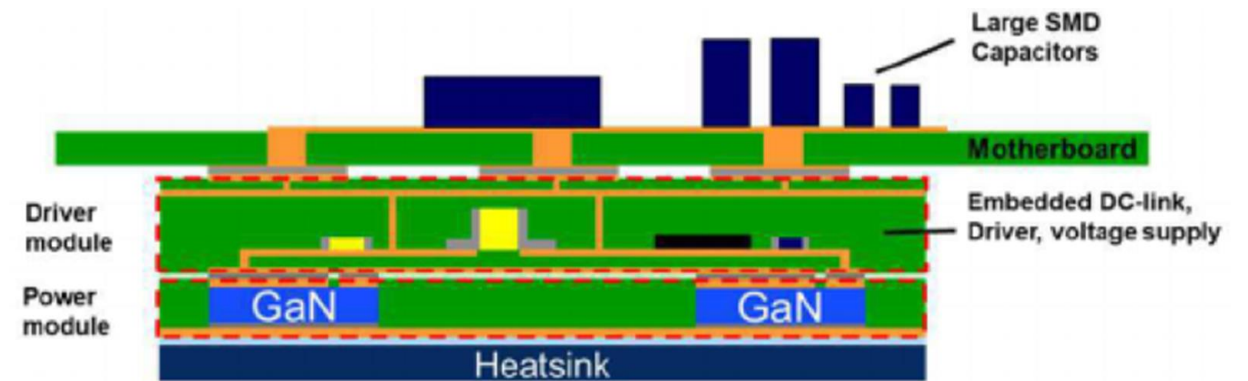
Power GaN Development Status & Trends

Key Optimization Directions for GaN-on-Si:

- Add epitaxial buffer layer; Process control of lattice mismatch during heterojunction growth, continuously optimize process, ensure yield;
- Strictly limit GaN max junction temp to 150°C (vs. SiC MOSFET 175°C), requiring more precise temperature measurement and circuit design;
- Implement complex double-sided cooling for GaN chip top and bottom, enhancing heat dissipation to prevent thermal degradation;
- Initially trade chip area, use D-mode GaN cascode MOS design (common-source/common-gate) for compatibility with existing gate drivers;
- Given these thermal challenges, PCB-embedded packaging is recommended, using chip-package co-design to solve GaN-on-Si HEMT application challenges;



D-mode GaN Cascode MOS Design
(Common-Source/Common-Gate)



GaN Chip Embedded Power Board
Packaging Design

Power GaN Development Status & Trends

GaN-on-Si BOM Cost Comparison:

- GaN-on-Si mainly uses Si substrate; required GaN epitaxial layer is only 5-7 μm .
- SiC is limited by vapor-phase epitaxy with low throughput, keeping substrate/epitaxy costs high with diminishing cost reduction trends;

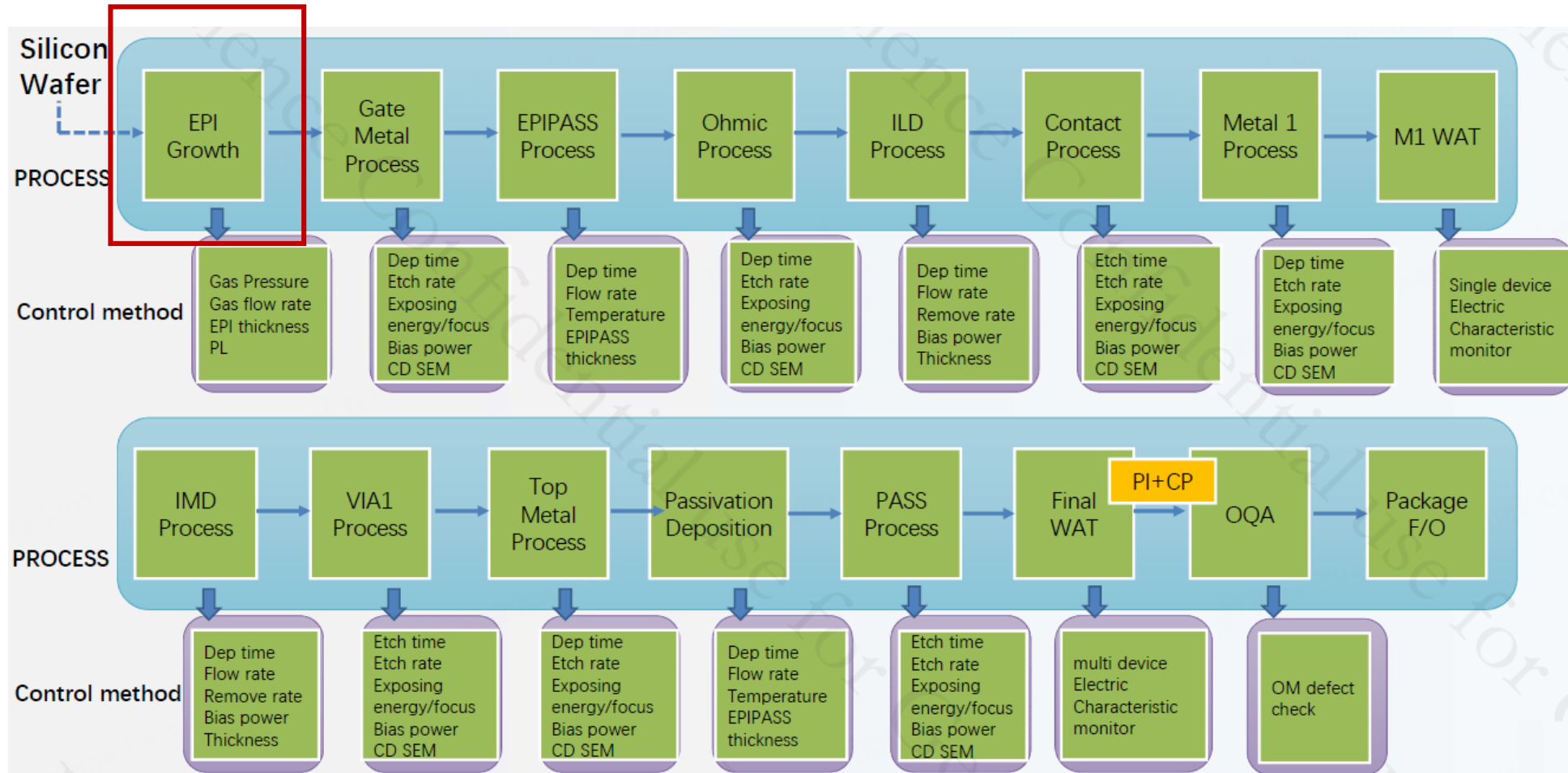


GaN vs SiC Chip Structure Comparison (Substrate + Epitaxy)

Power GaN Development Status & Trends

GaN-on-Si Process Cost Comparison:

- GaN-on-Si uses Si substrate; except for epitaxy, production flow is essentially identical to Si devices, with comparable process cost potential.



Si-based GaN Main Process Flow:
Processes other than epitaxial growth are essentially
same as Si MOS

Power GaN Development Status & Trends

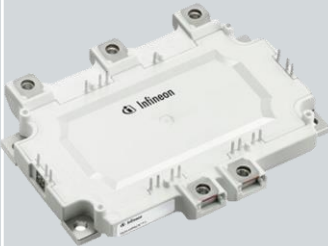
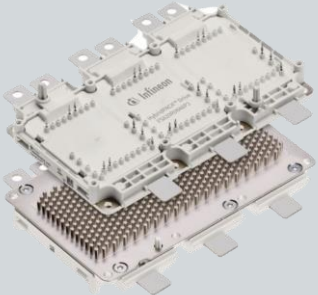
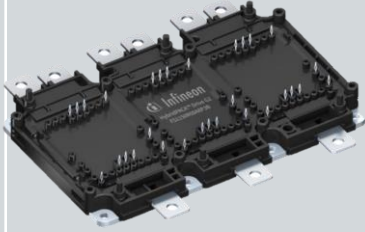
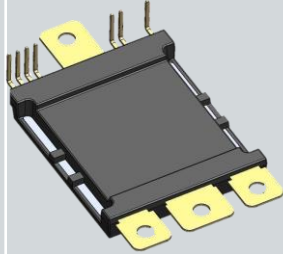
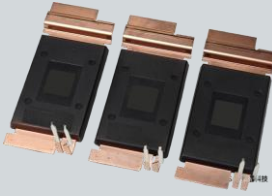
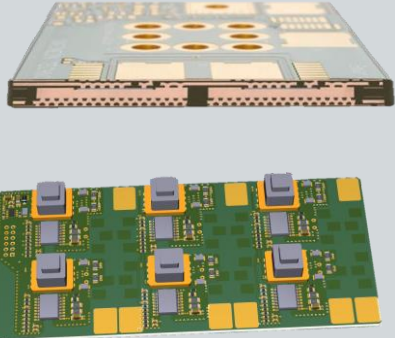
GaN-on-Si Comprehensive Cost Prediction Model:

- GaN-on-Si uses Si substrate with only 5-7um GaN epitaxy; production flow matches Si devices. Considering specific current cost, GaN theoretical cost floor is only 40% of Si devices;

Item		Si Device Cost Structure	SiC Device Cost Structure	GaN-on-Si Device Cost Structure	Notes
Raw Materials	Base Materials	Si: 300-400 CNY/ton (1.0)	■ Si: 300-400 CNY/ton ■ C: 100 CNY/ton (1.0)	Si: 300-400 CNY/ton N: 450 CNY/ton (1.2) Ga metal: 1,690,000 CNY/ton	
	Total Raw Material Cost	1.0	1.0	1.2	GaN epitaxy is 5-7um, so raw material cost is ~1.2x Si devices
Processing	Substrate Crystal Growth Rate	1	200	20	GaN-on-Si only grows epitaxy, so total crystal growth time is only slightly more than Si
	Wafer Processing Cost	1	40	1.2	
	Raw Material & Manufacturing Cost Comparison	4:1	1:10.2	4:1	
Total Cost	Total Raw Material & Manufacturing Cost	1	8.96	1.2	
Cost per Performance	Current Capability	1	5	3	GaN high-temp current capability slightly below SiC, but still better than Si
	Device Cost per Current Unit Comparison	1	1.8	0.4	

Power Electronics Packaging Status & Trends

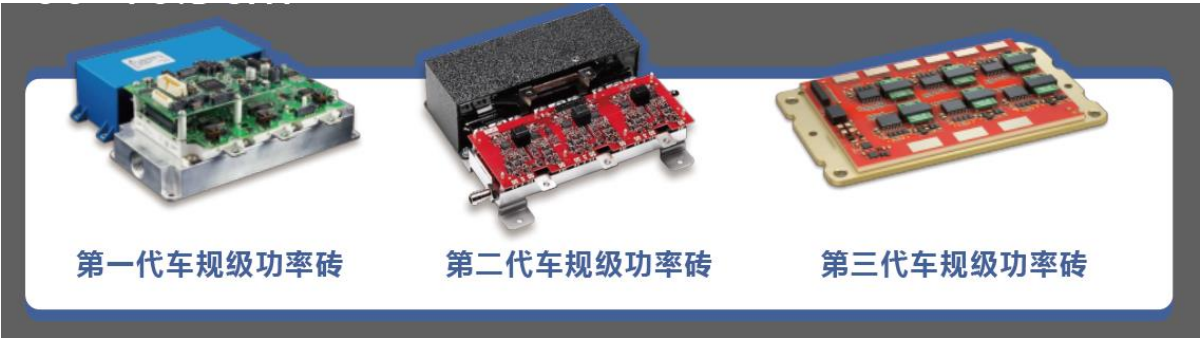
- Automotive power semiconductor packaging has evolved through ~3 generations: 1st gen (Plastic Case), 2nd gen (Molded); and possible 3rd gen (PCB-embedded?);
- Plastic case and molded packages are in mass production. PCB-embedded is not yet in production but under active R&D; mass production expected by 2027-28.

	1st Gen: Plastic Case Packaging			2nd Gen: Molded Packaging		3rd Gen: Embedded Packaging?
Representative Mfr.	Infineon			Danfoss	STMicroelectronics	ZF
Part Name	HP1	HP2 G1	HP2 G2	DCM	TPAK	CIPB
Legend						

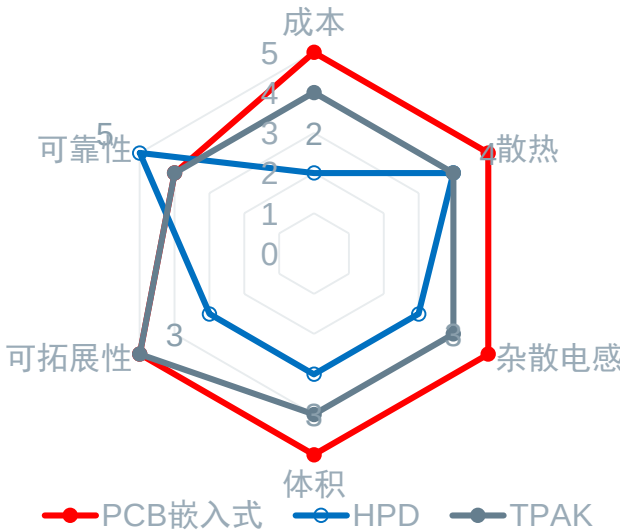
Power Electronics Packaging Status & Trends

Power Device Packaging Comparison

- PCB-embedded modules show significant advantages in cost, thermal, stray inductance, and volume;
- But high-voltage high-power parallel process reliability needs validation;



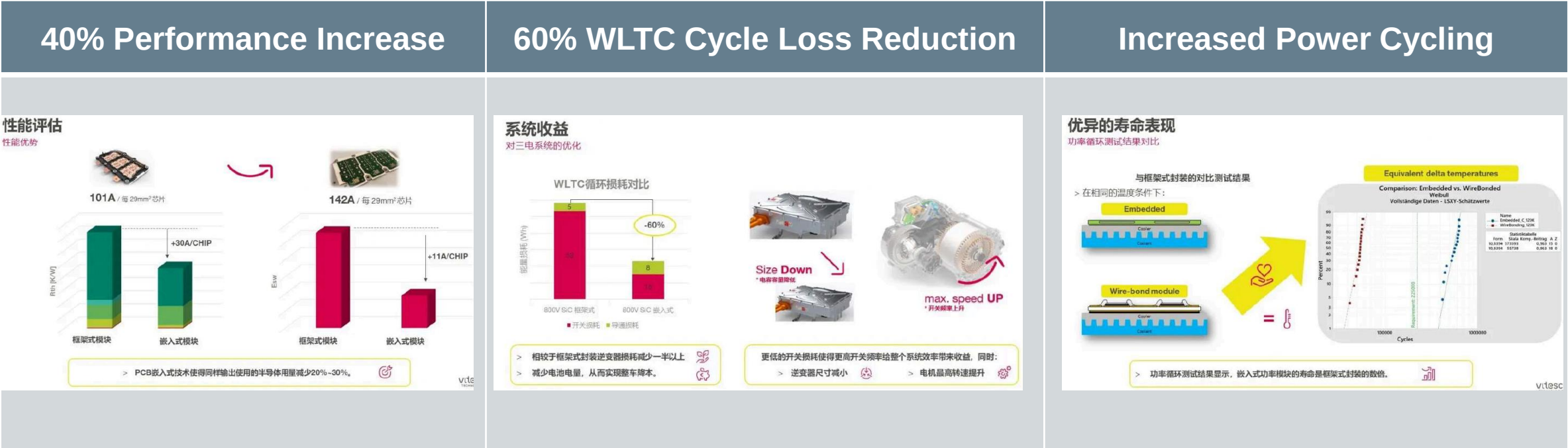
Embedded vs. Traditional Module Performance		HPD Package	TPAK Package	PCB Embedded Power Module
Power Module	Switching Loss	HPD>TPAK>PCB Embedded		
	Thermal Resistance Rth J-C	0.1 - 0.4K/W	0.1 - 0.4K/W	0.1 - 0.4K/W
	Stray Inductance	7 - 14nH	4 - 8nH	<2nH
	System Power Density	15 - 50kW/L	20 - 60kW/L	60 - >>100kW/L
System	Integration Level	Low	Low	High (Power + Control Circuit Integration)
	Cycle Reliability	HPD>TPAK~PCB Embedded?		
Cost	Packaging Cost (excl. chip)	HPD>TPAK>PCB Embedded		



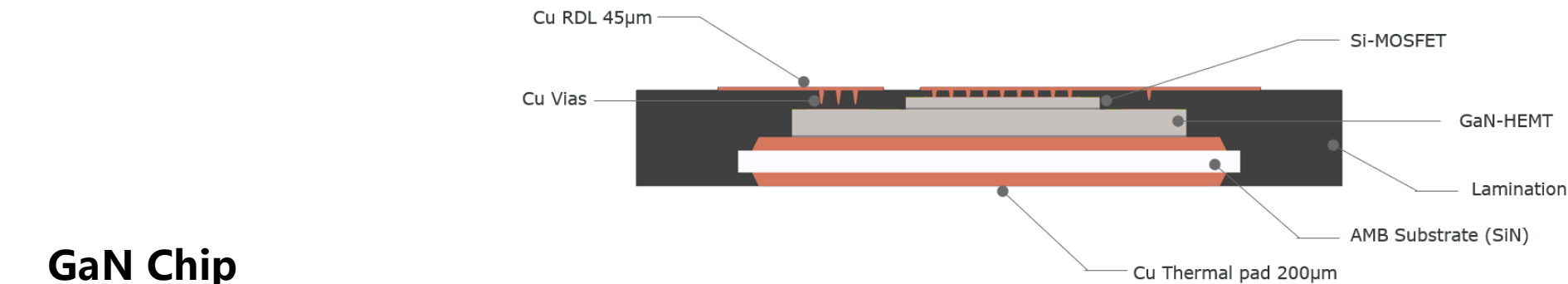
Power Electronics Packaging Status & Trends

PCB Embedded Packaging Advantages

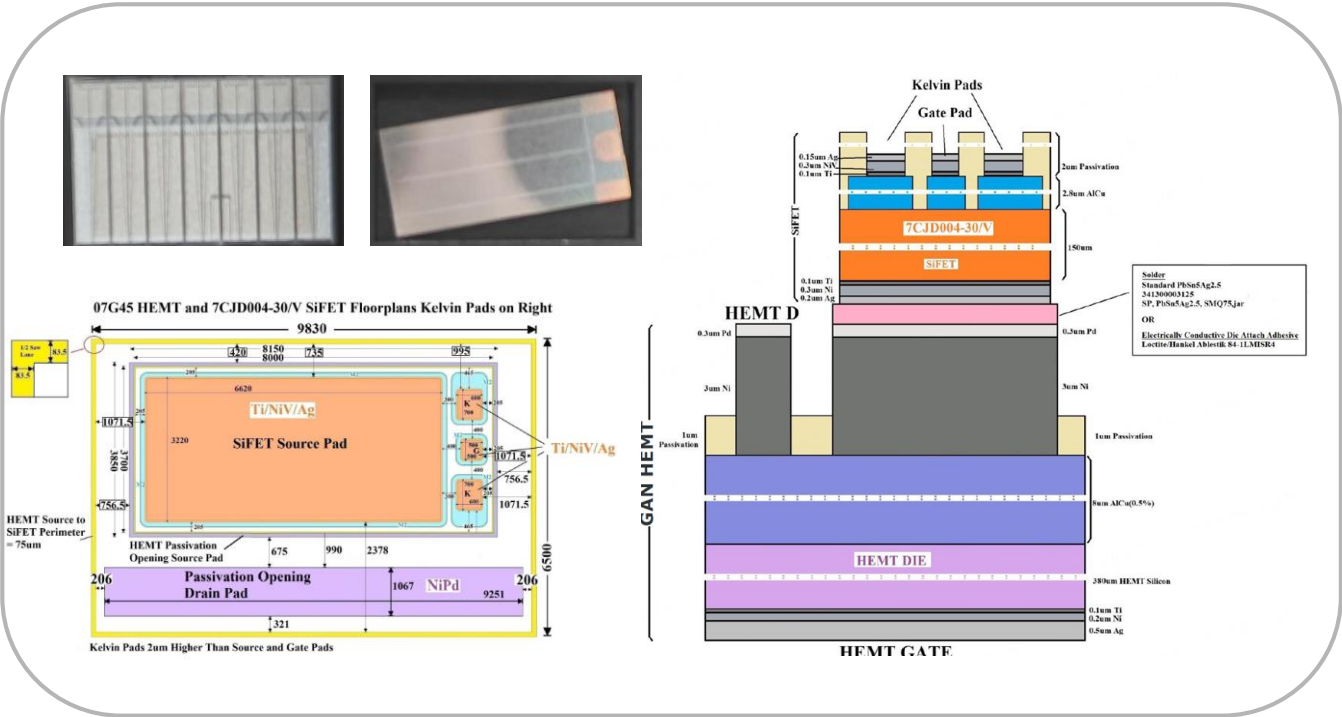
- 2024 Vitesco analysis: vs. traditional packaging, PCB-embedded modules improve current density by ~40%, or reduce semiconductor usage by 1/3 at same current; BOM cost may drop 20% at same power output.
- PCB-embedded commutation loop stray inductance can be reduced below 1nH, cutting inverter switching loss to 1/3 of traditional products, so frequency-related loss increase is reduced by 2/3.



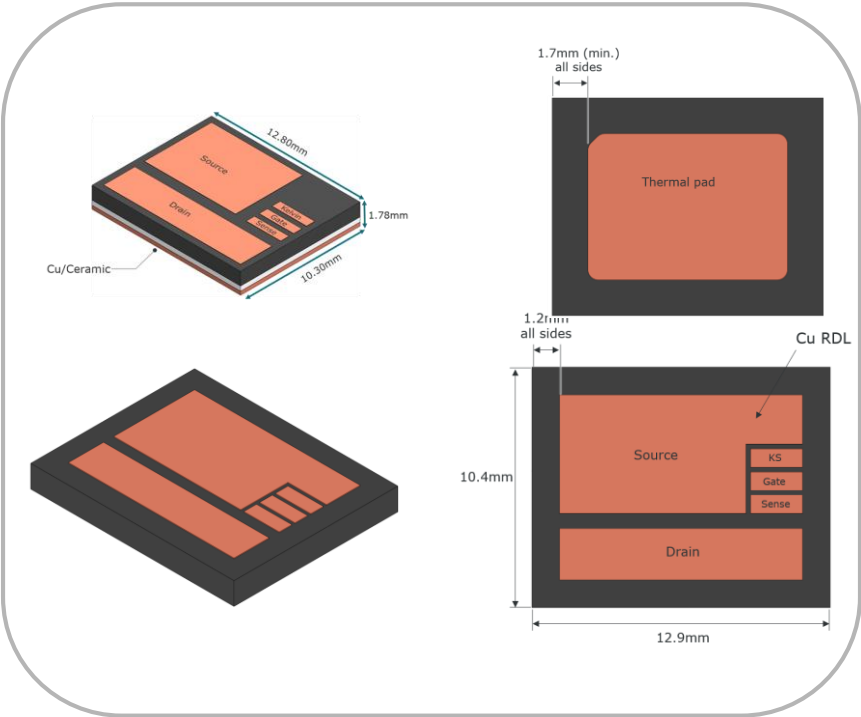
HORSE PCB Embedded GaN Power Module Design



GaN Chip



GaN CELL

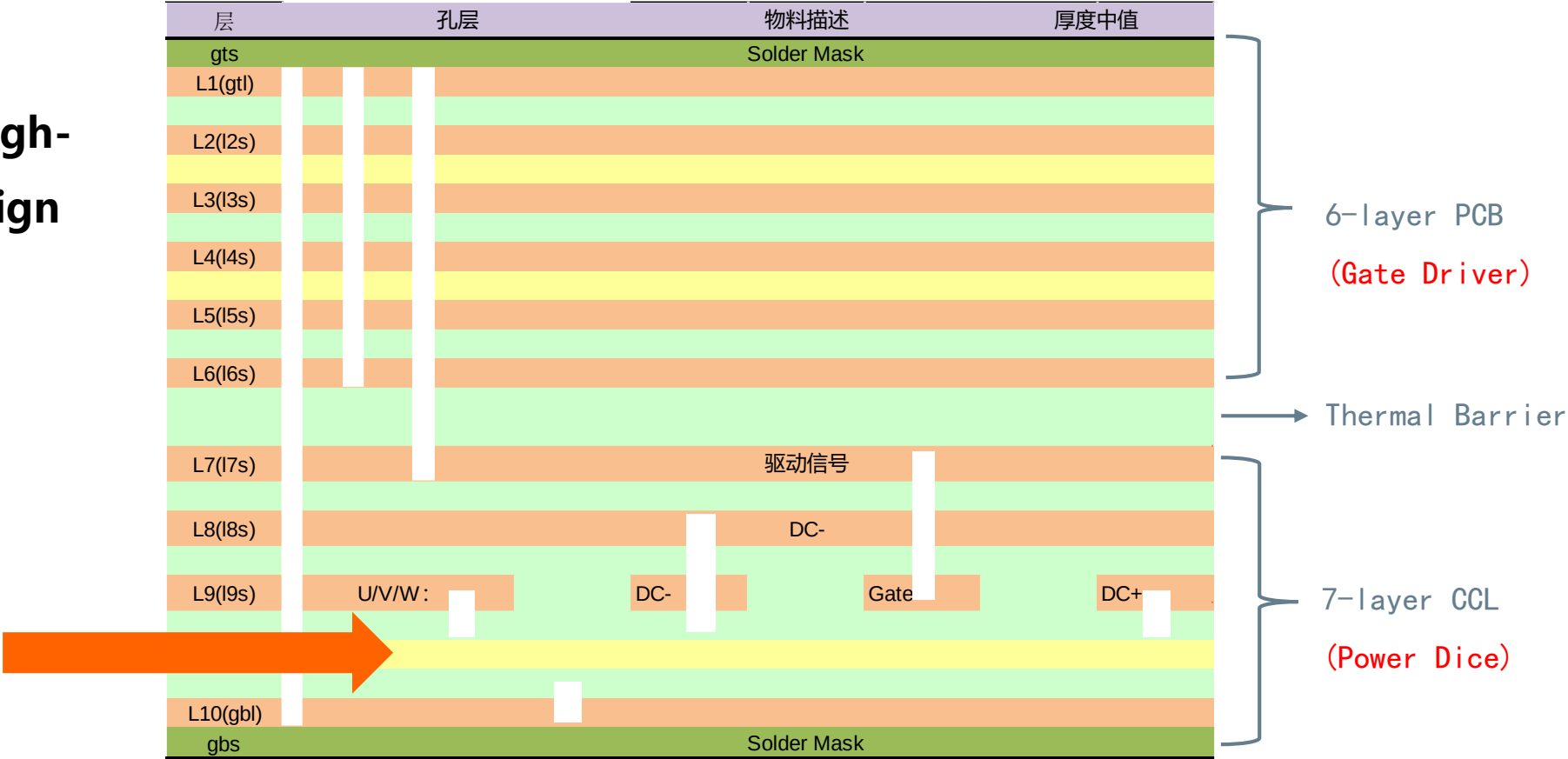
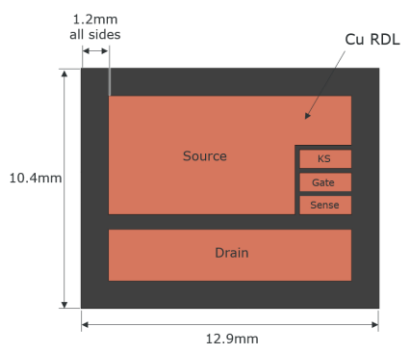


D-mode Cascode Stacked Chips Structure

Stacked Molded AMB Cell

HORSE PCB Embedded GaN Power Module Design

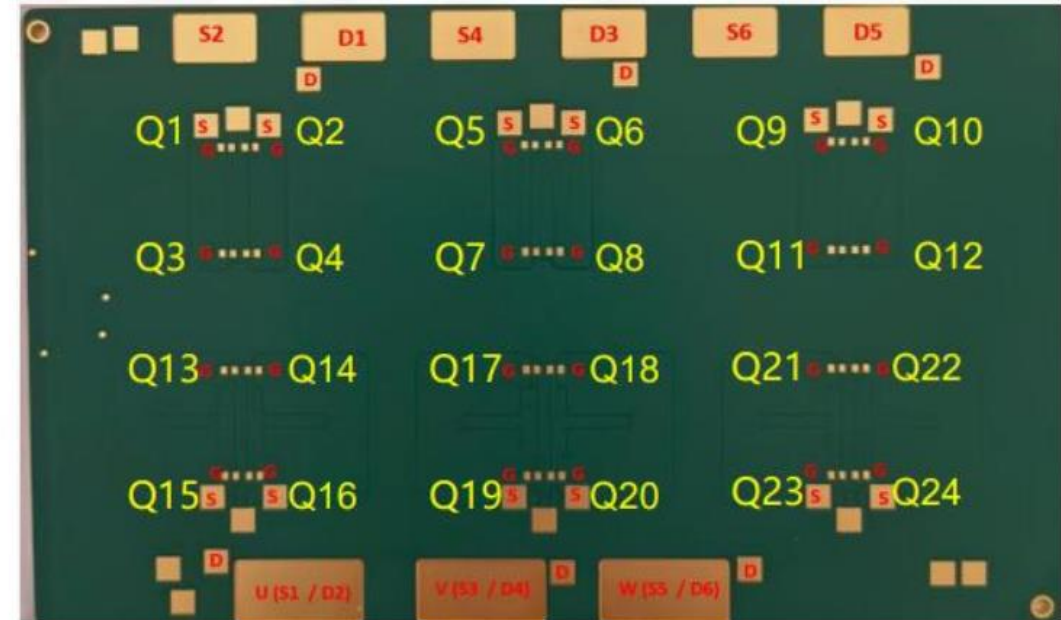
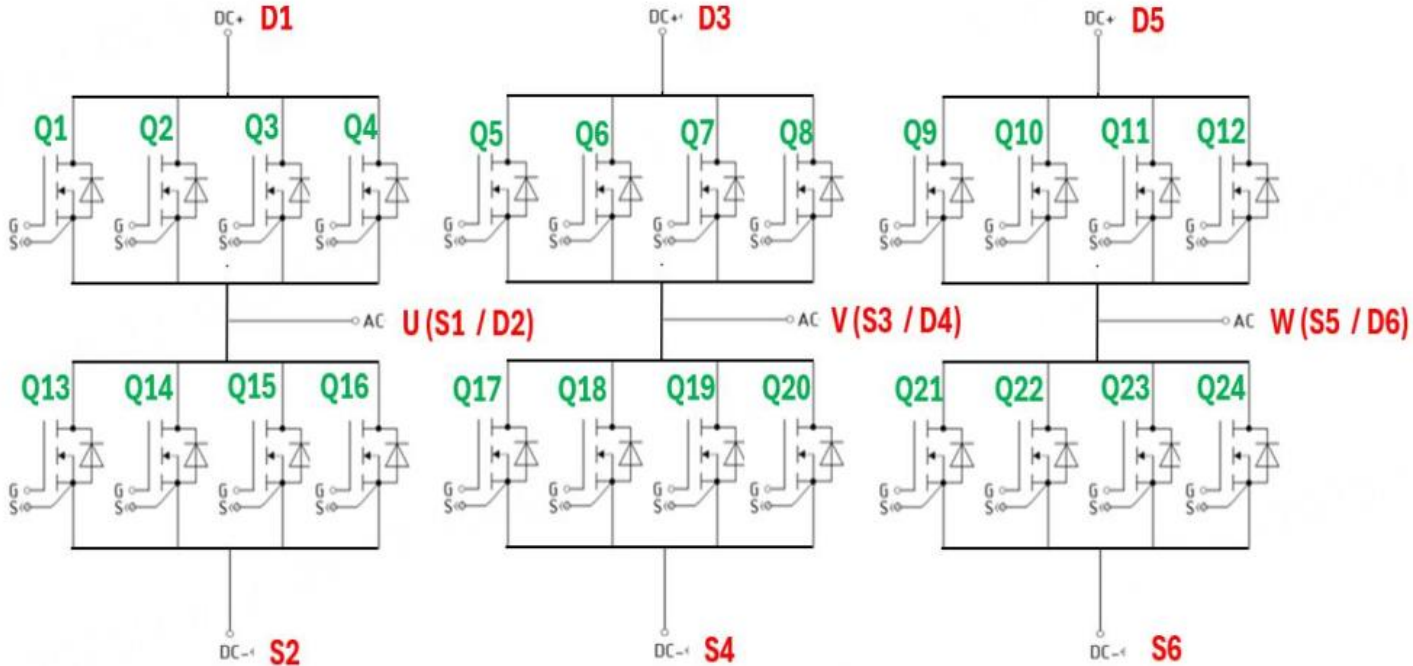
■ Molded Cell + Driver
Integrated Multi-layer High-density PCB Stackup Design



14-layer Laminated Embedded Board Stackup Design

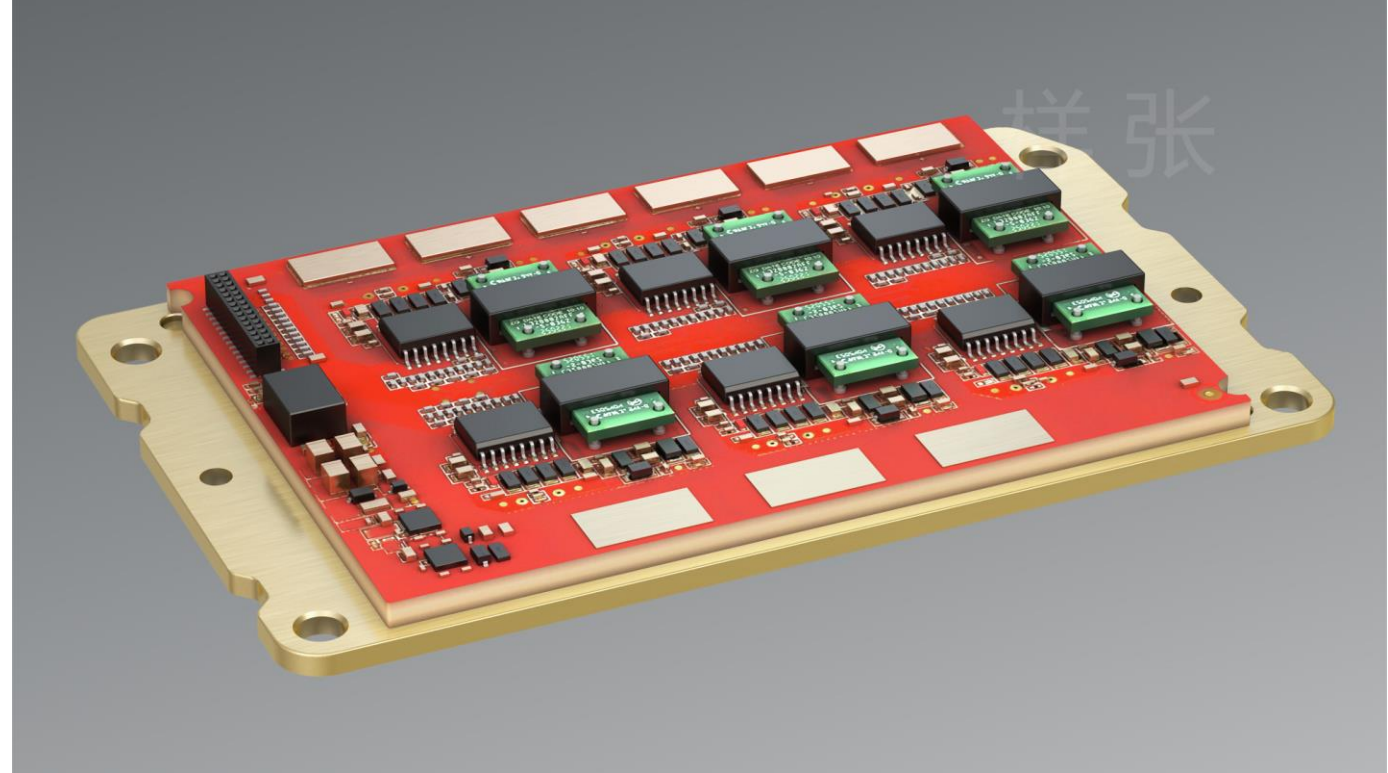
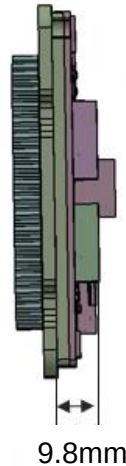
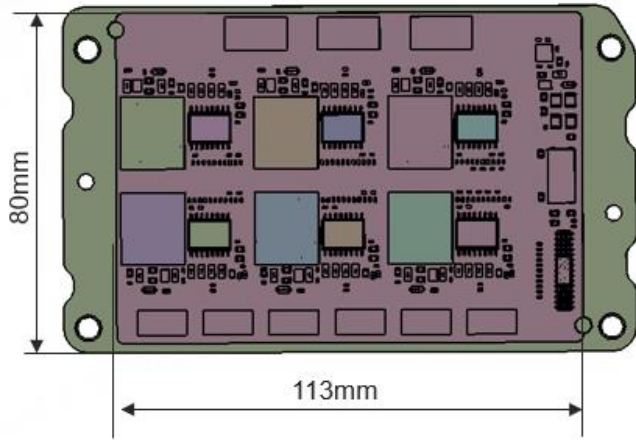
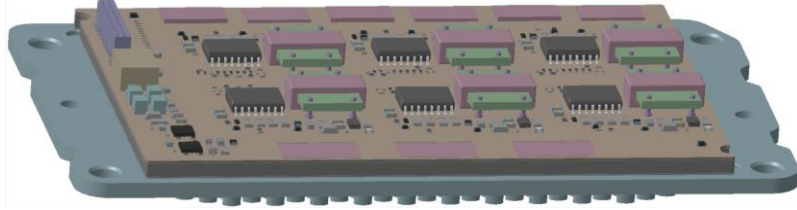
HORSE PCB Embedded GaN Power Module Design

■ High-Voltage High-Power GaN Chip Parallel Embedded Layout



HORSE PCB Embedded GaN Power Module Design

■ “IceBlade” Power Module

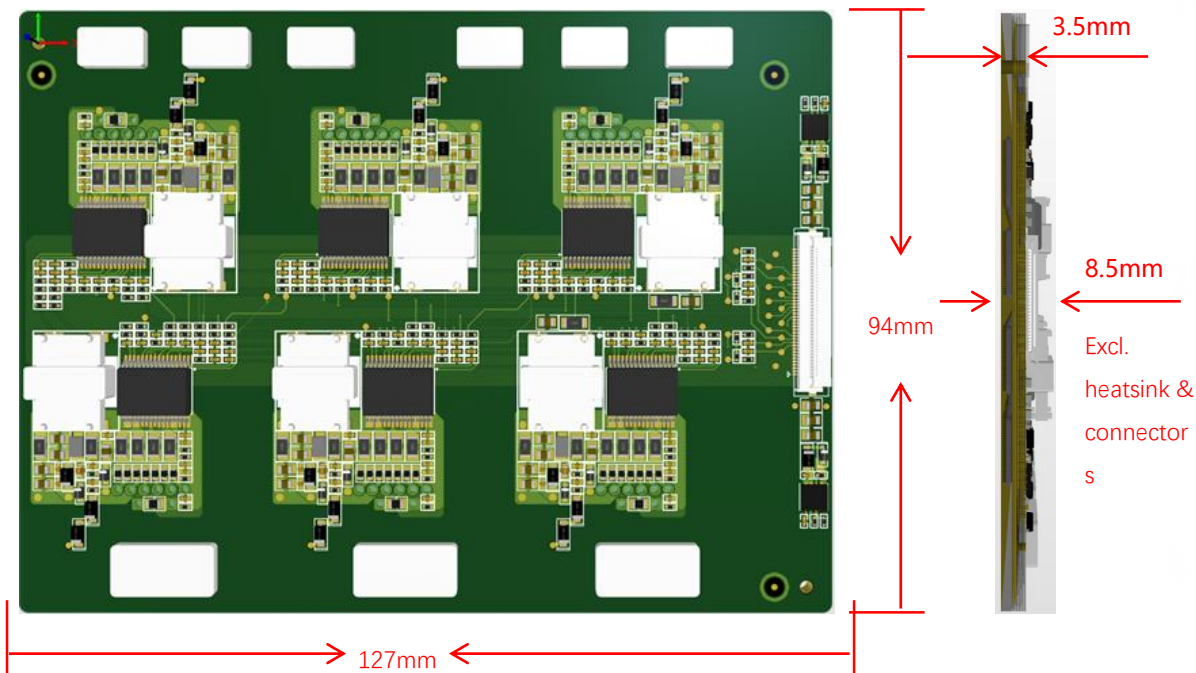


- Overall height reduced 35%, volume >50%, stray inductance >90% to 1nH vs. existing modules, industry-leading;
- The “IceBlade” series power modules can achieve a power density of up to 685 kW/L or 294 kW/kg;
- Reduced losses, enhanced cooling >20% efficiency, improved controller pulse current output;
- Traction inverter WLTC avg. efficiency +2%; volume -40%;

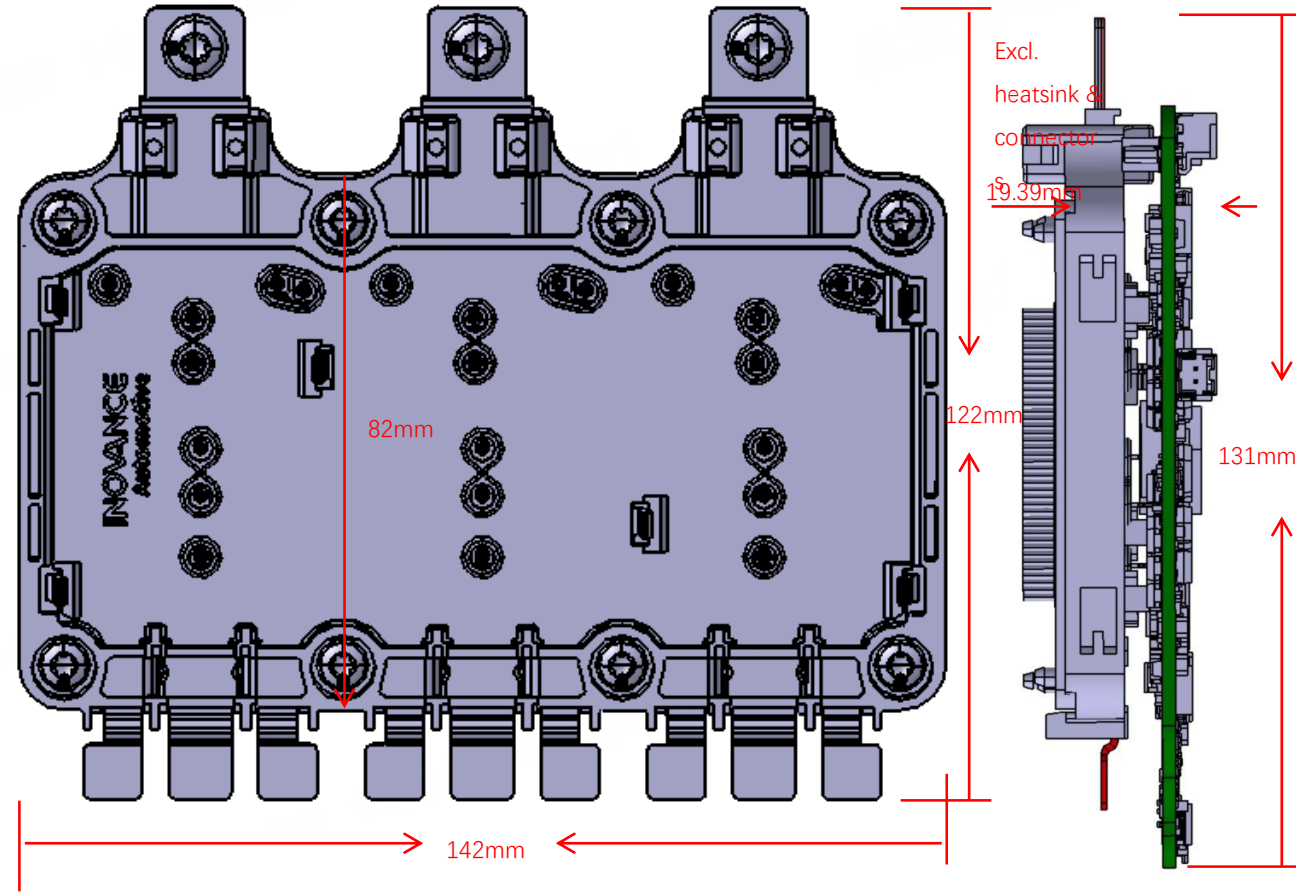
HORSE PCB Embedded GaN Power Module Design

■ PCB Embedded Power Module for X-in-1 Control Module (XCM) of HORSE Hybrid

Embedded module platformization: P1 and P3 modules share components and stackup.



mXCM P3 Embedded Module (400V)



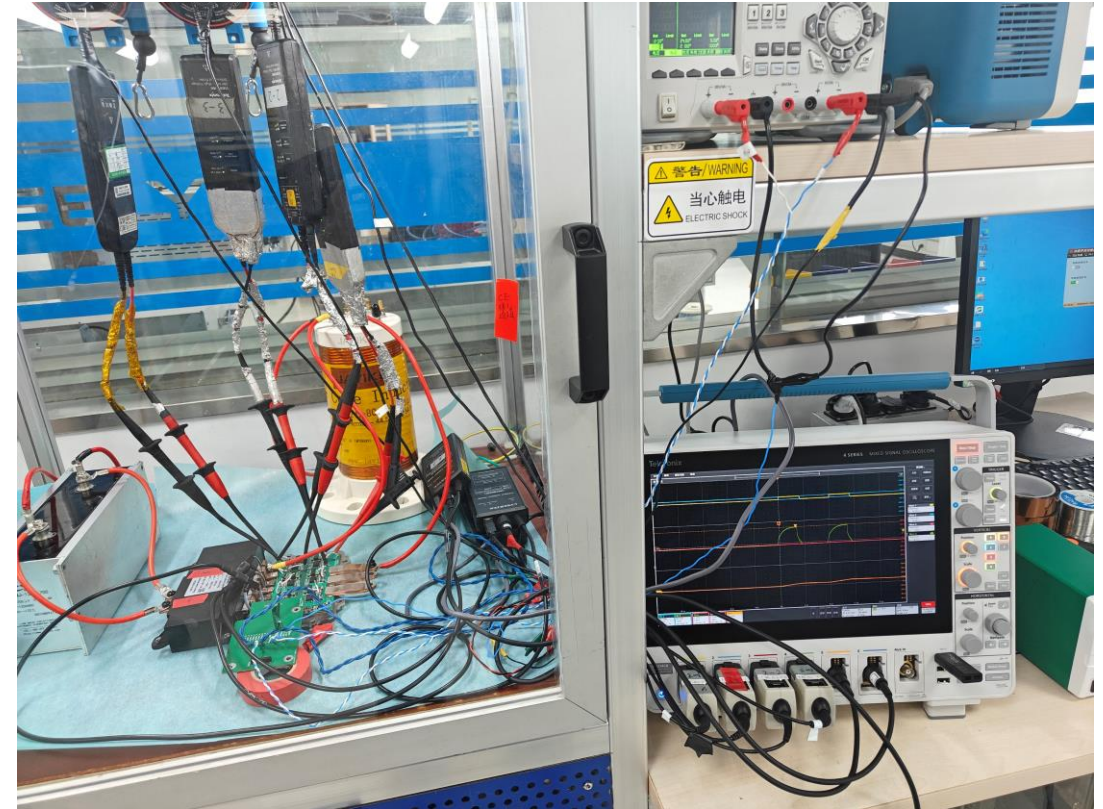
Existing P3 Module (400V)

HORSE PCB Embedded GaN Power Module Design

■ Testing of “IceBlade” Power Module



Double Pulse Test Module

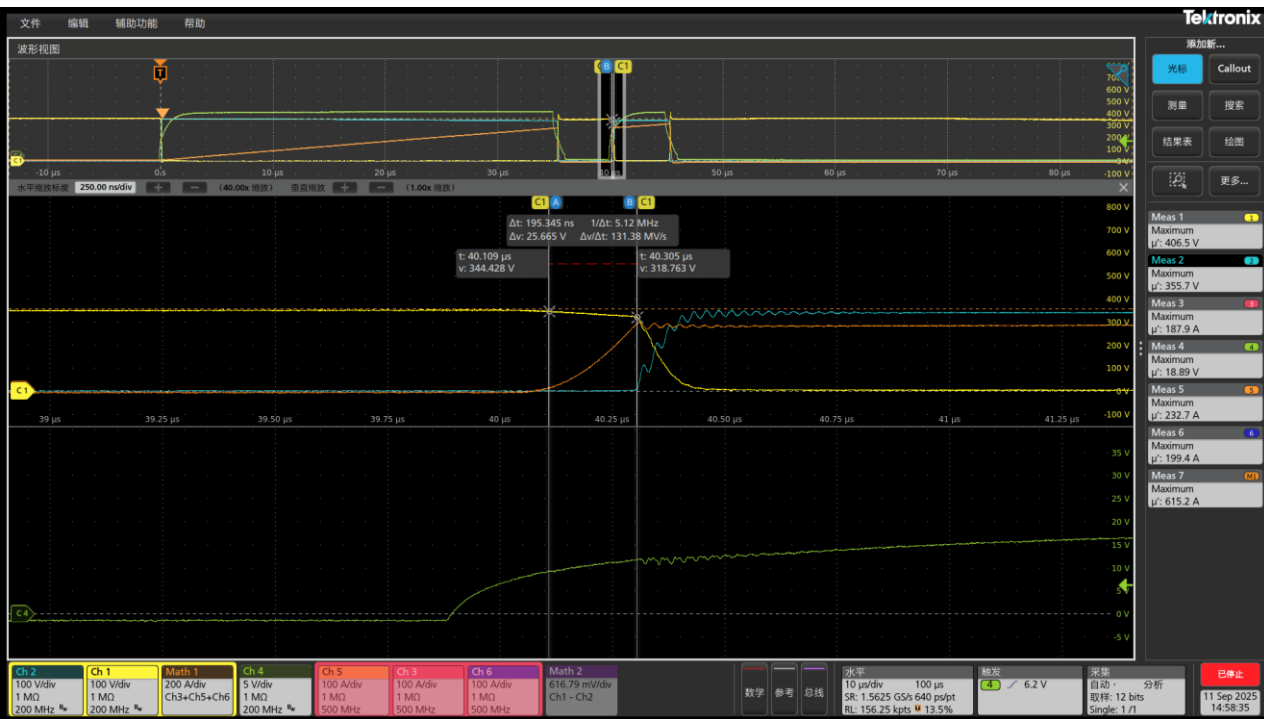


Double Pulse Test Bench

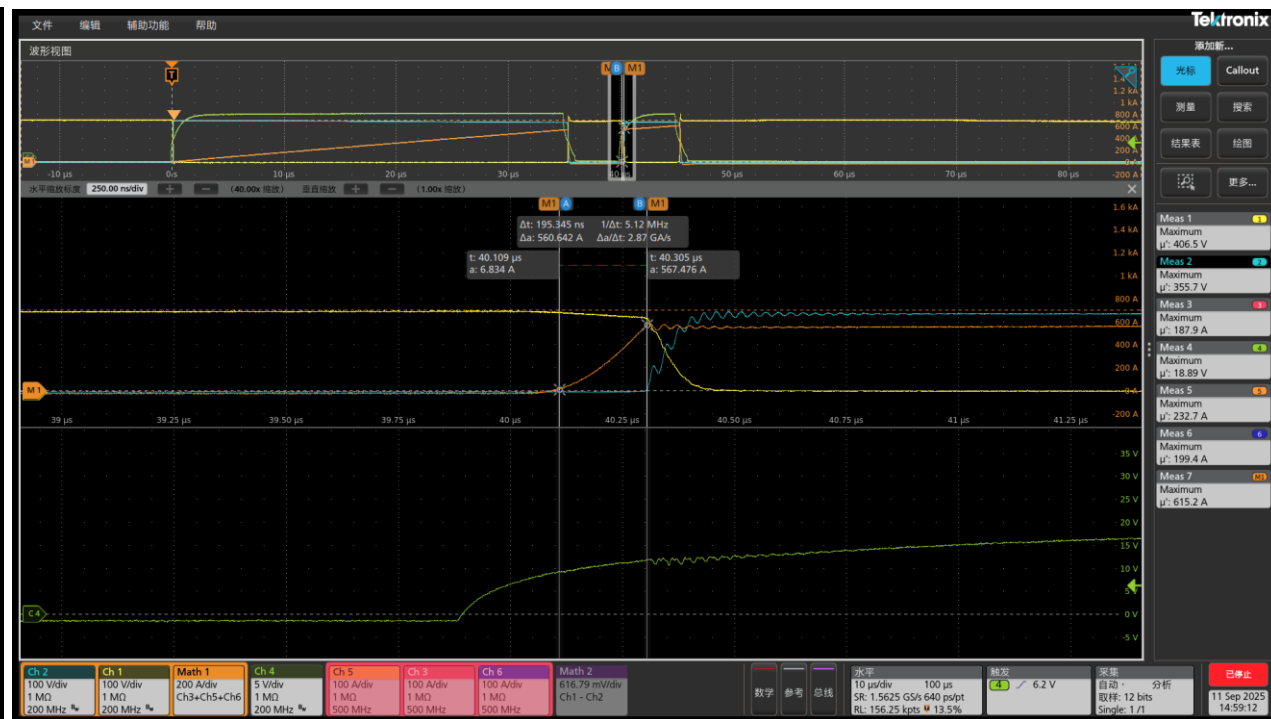
HORSE PCB Embedded GaN Power Module Design

■ Testing of “IceBlade” Power Module

◆ Upper arm of bridge: bus 350V, $dU=25.6V$, $dt=195.3ns$, $dI=560A$; system stray $L=U \cdot t / I = 8.928nH$ (incl. $\sim 6nH$ capacitor stray L),



$\Delta U=25.6V$, $\Delta t=195.3ns$



$\Delta I=560A$

CH4: Upper GS
Math 1: Current
CH1: Upper DS
CH2: Lower DS

HORSE PCB Embedded GaN Power Module Design

■ Testing of “IceBlade” Power Module

- ❑ “IceBlade” embedded module advantage up to **41.02%** vs. existing competitors;
- ❑ Drive optimization: $R_{gon}=1\Omega$; $R_{goff}=2.8\Omega$

● Traditional Pkg. Loss

HD18	Test Conditions	UNIT	HD18 2-par 32mm2 UL
$t_{d(on)}$	$V_{CE}=935V, I_C=375A,$ $V_{GE} = -5V/+18V,$ $C_{gs}=10nF,$ $H:R_{gon}=6.2\Omega,$ $R_{goff}=7.2\Omega$ $L:R_{gon}=10\Omega,$ $R_{goff}=2.7\Omega$ $T_{vj}=25^\circ C$	ns	155
t_r		ns	142
$t_{d(off)}$		ns	163
t_f		ns	64
$di/dt(on)$		A/us	2114
$dv/dt(off)$		V/us	29170
E_{on}		mJ	35.6
E_{off}		mJ	14.2
E_{tot}		mJ	49.8
$V_{F_{peak}}$		V	991
V_{cepeak}		V	1186
I_{RM}		A	35
E_{rec}		mJ	0.06

● Embedded Pkg. Loss

V-phase lower, 995V			
	Unit	$R_{goff}=2.8,$ $R_{gon}=1, \text{ rear } 6 \times 6\Omega \text{ parallel}$	
		375A	800A
E_{on}	mJ	15.43	35.41
E_{off}	mJ	13.94	37.17
E_{tot}	mJ	29.37	72.58
$V_{F_{Peak}}$	V	1070	1071
V_{cePeak}	V	1126	1191

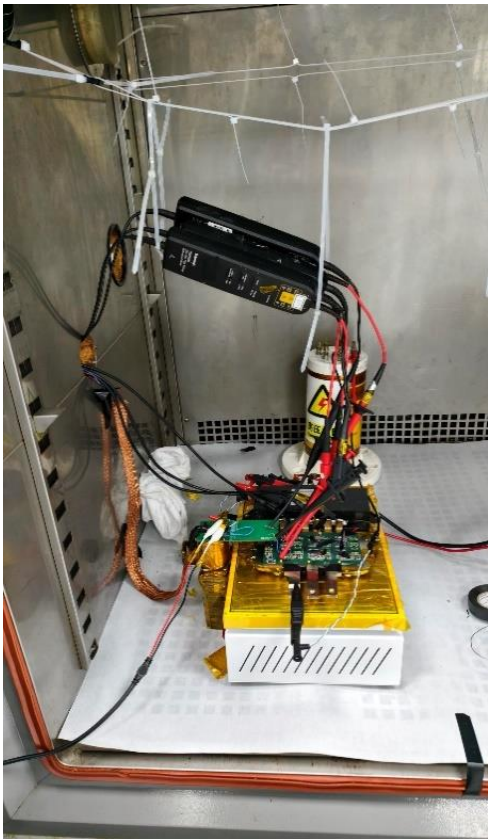
● Loss Comparison vs. Traditional

$I_C=375A$	Traditional I Pkg.	Horse Embedded	Delta
E_{on}	35.6	15.43	-56.6%
E_{off}	14.2	13.94	-14%
E_{tot}	49.8	29.37	-41.02%

HORSE PCB Embedded GaN Power Module Design

■ Testing of “IceBlade” Power Module

➤ After subtracting capacitor stray, embedded module stray <2nH



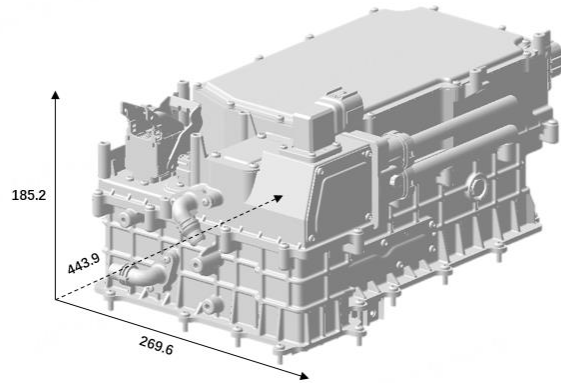
Test current 900A				
	Turn-on Time (μs)	System Stray (nH)	Capacitor Stray (nH)	Module Stray (nH)
UH	2.5	7.3	6.4	0.9
UL	2.5	8.2	6.4	1.8
VH	2.5	6.81	6.4	0.41
VL	2.5	7.67	6.4	1.27

HORSE Next-gen X-in-1 Hybrid Controller (XCM) Design

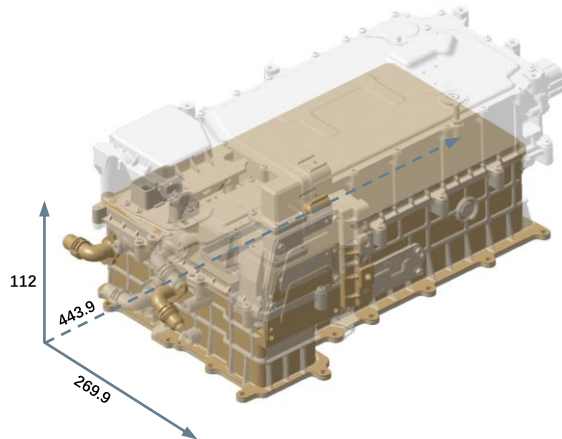
■ Design Target

➤ Volume target: **>40%** reduction vs. current XCM platform.

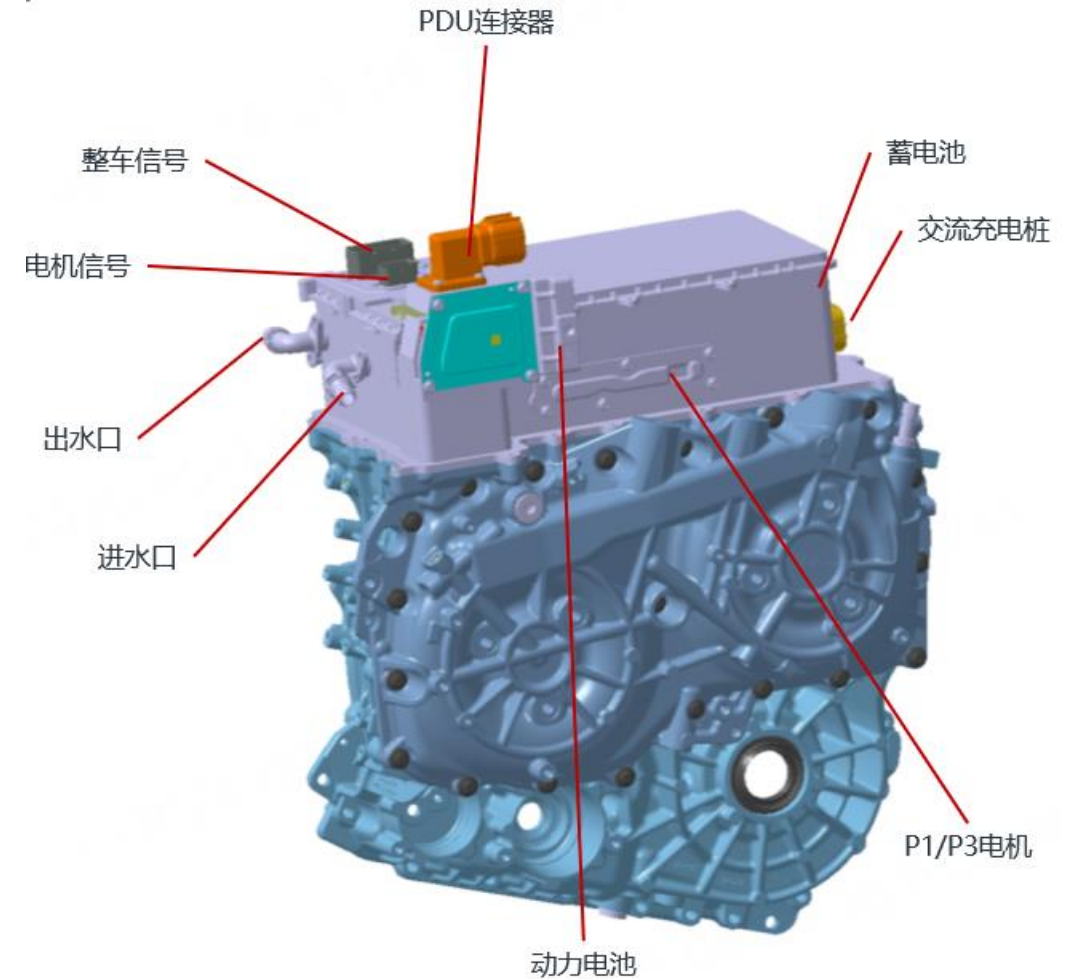
- Current XCM: 18.2L



- Next-gen mXCM Target: $\leq 10.92\text{L}$



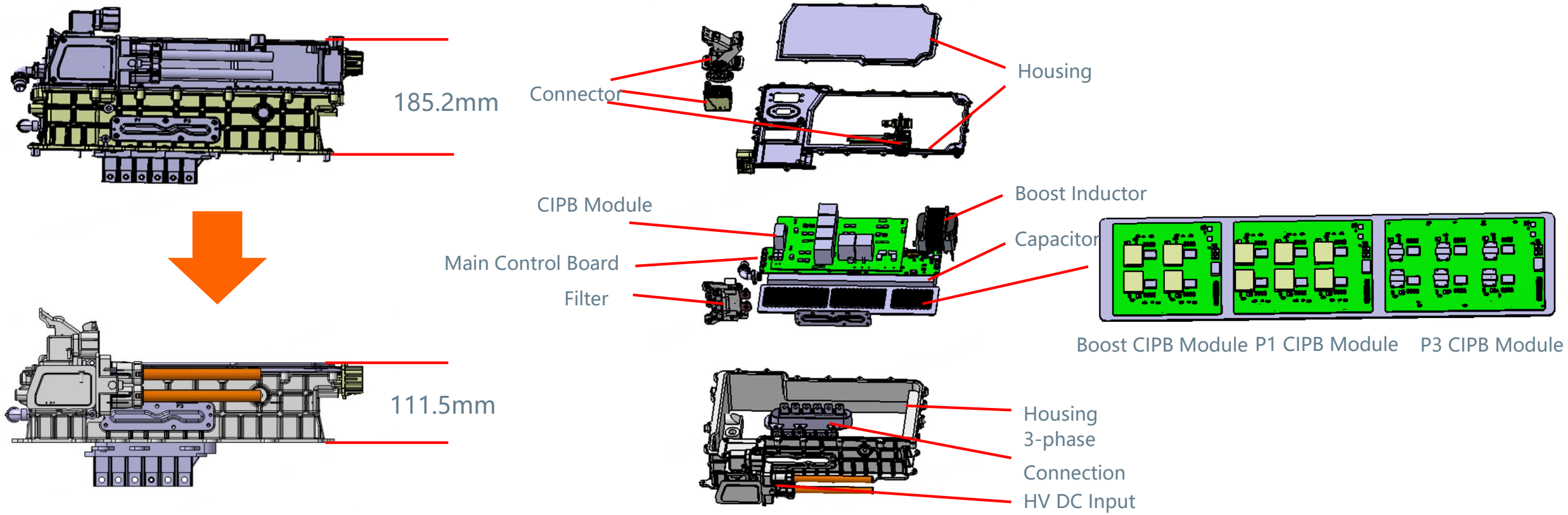
■ Overall Layout of Hybrid System



HORSE Next-gen X-in-1 Hybrid Controller (XCM) Design

■ Internal Structural Layout

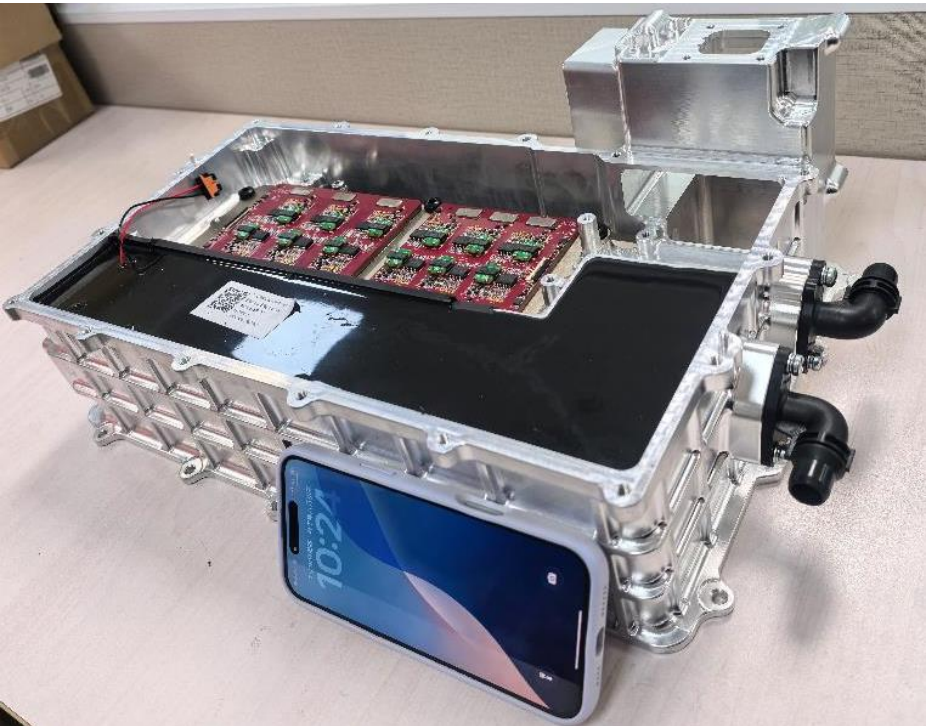
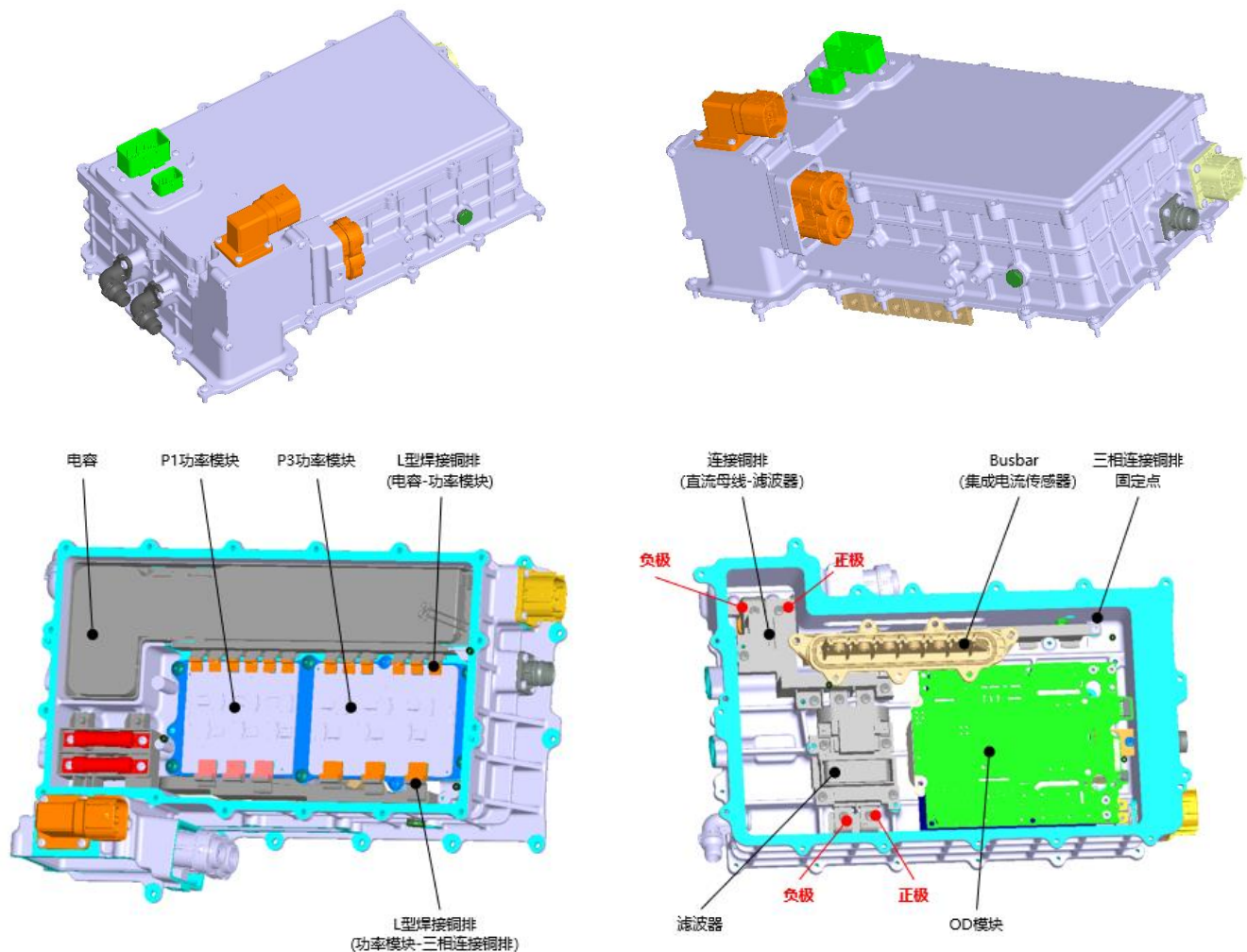
- By integrating power devices with gate-driver PCB, XCM modules reduce Z-dimension by 40%.



XCM Layout

HORSE Next-gen X-in-1 Hybrid Controller (XCM) Design

■ Next Gen hybrid mXCM Prototype

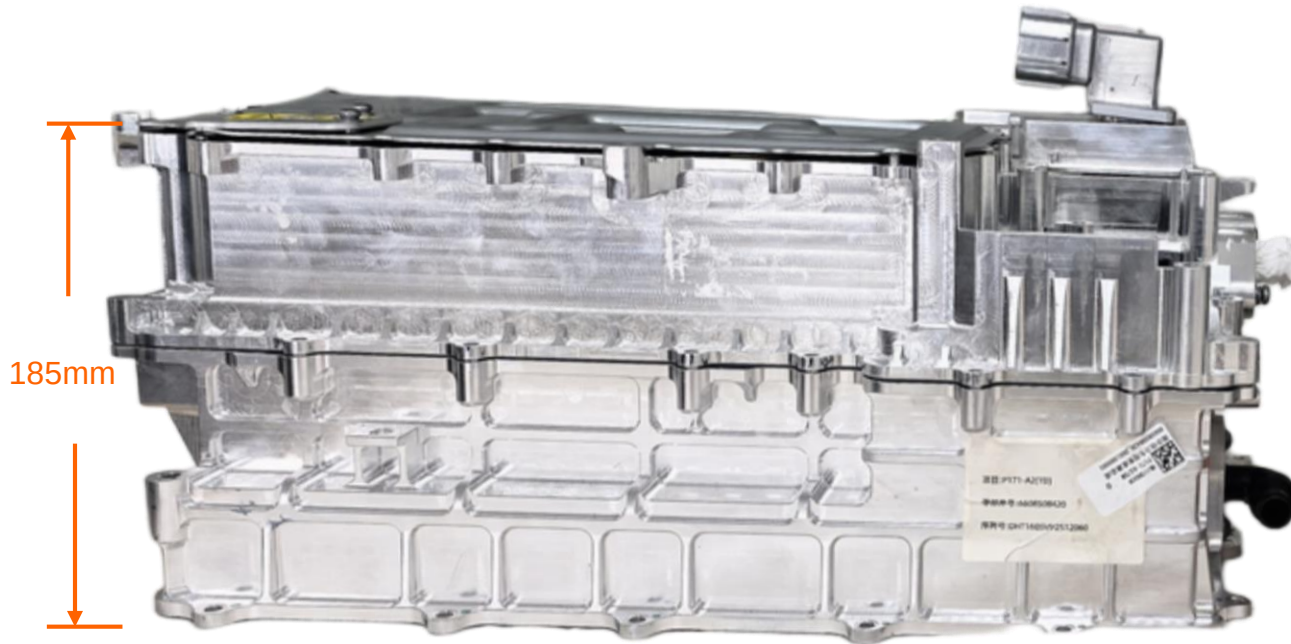


HORSE Next-gen X-in-1 Hybrid Controller (XCM) Design

■ Next Gen hybrid mXCM Prototype

Finally 44% height & volume reduction achieved vs. existing XCM

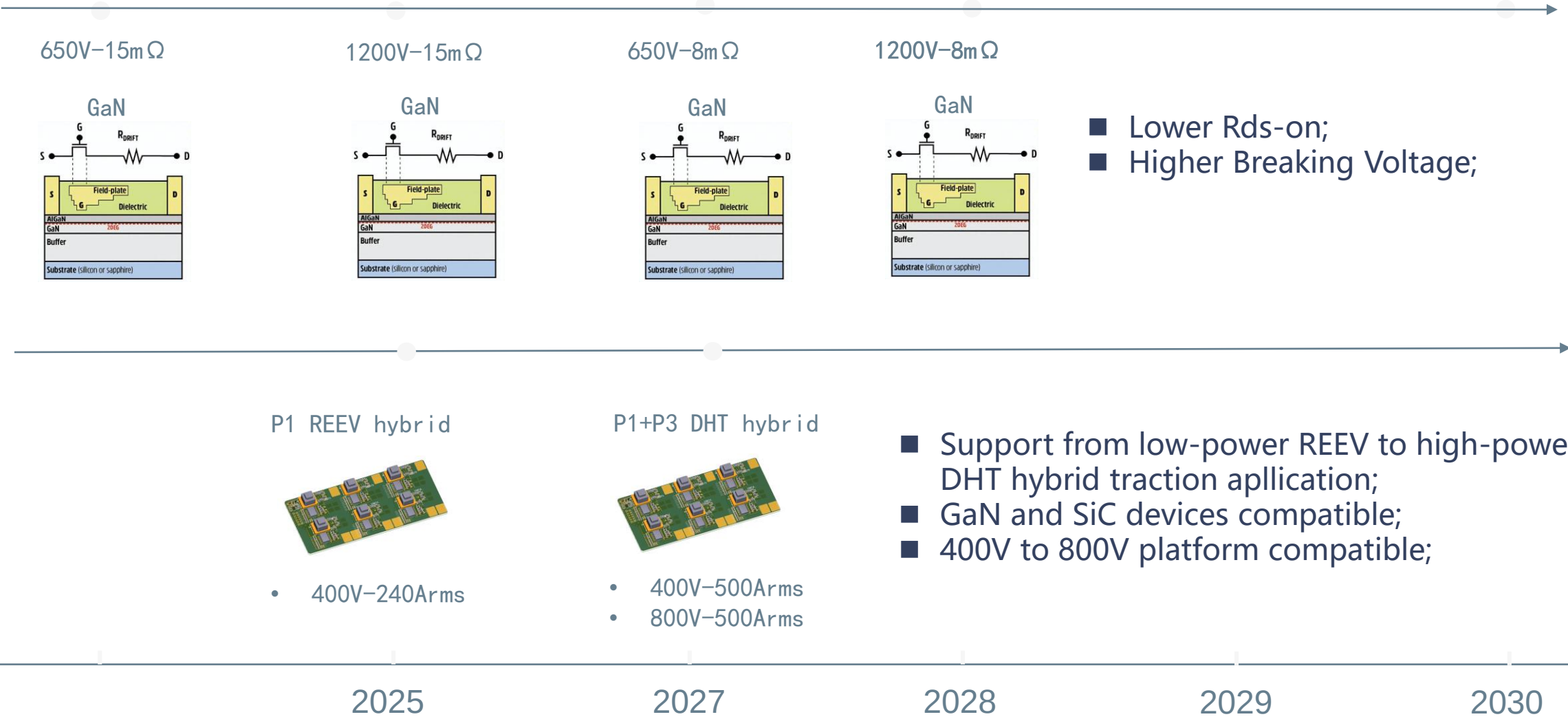
Existing XCM



Next-gen mXCM Prototype



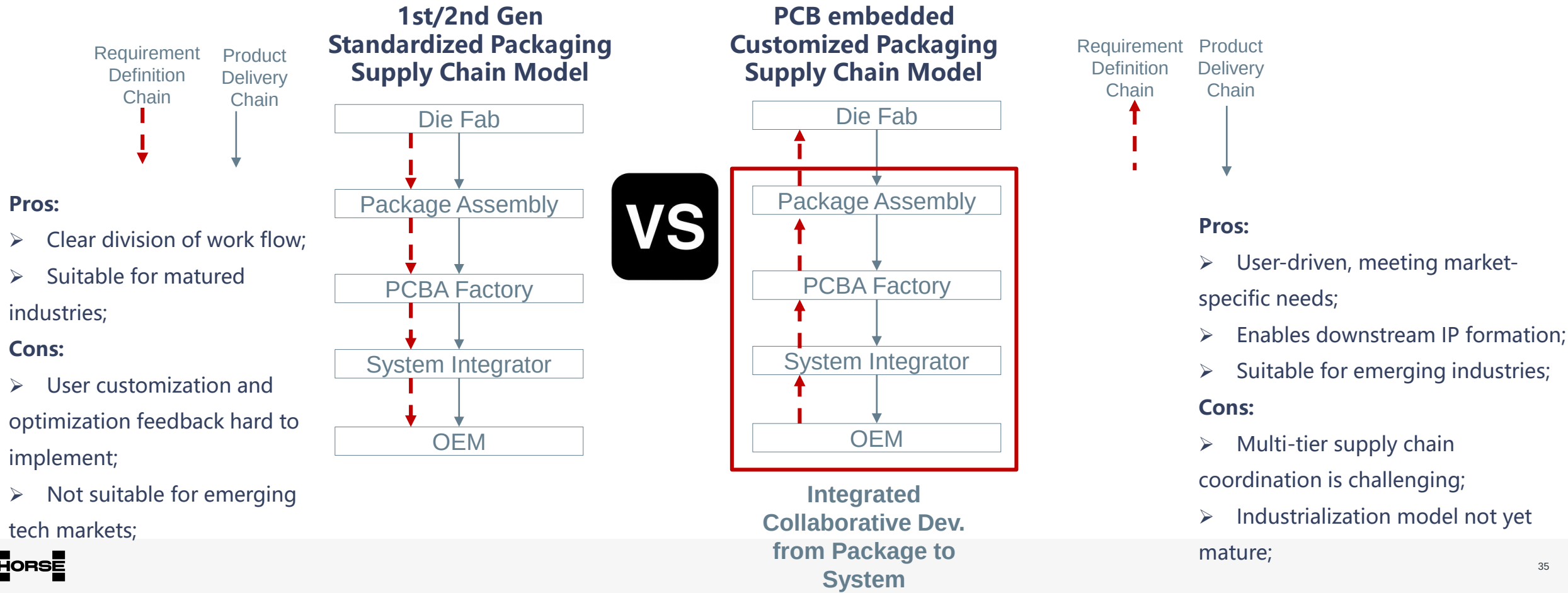
Outlook: HORSE Embedded POWER Module Roadmap



Outlook: Impact on Automotive Power Electronics Supply Chain

Power semiconductor packaging evolution drives automotive power electronics industry chain transformation

- 1st/2nd gen packaging is standardized design, single-trip forward delivery with clear work-flow division but no continuous end-user feedback; **open-loop supply chain**;
- PCB embedded packaging is customized design, enabling customer-involved collaborative development; **close-loop supply chain**;





Achieving Net-Zero: Pure Electric Is Not the Only Path

THANK YOU

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